Low-cost Compact Approach to Reinforced Isolated Drive for LLC Converters

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***Abstract*— Modern power converters are expected to have high efficiency and features like datalogging. This typically results in a design with a digital controller implemented on the secondary side, which means having to drive transistors across the galvanic isolation barrier. The most common approaches are a) Bulky magnetic drive with many turns of triple-isolated wire; b) Compact but costly coreless transformer ICs that also require local powering; This work presents an alternative approach, which optimizes size and cost without compromising performance in traditional applications, intended for driving a complementary pair of MOSFETs like in Half-Bridge LLC converters.**

Keywords—isolated gate driver, floating gate driver, half-bridge gate driver.

I. INTRODUCTION

A typical Half-Bridge (HB) LLC converter [3] has two 600V transistors on the primary side that are driven with 50% duty cycle in a complementary fashion. With the controller situated on the secondary side, the drive signals must be conveyed across the isolation barrier [8]. Driving transistors across the isolation barrier can be split into three categories based on the principal of operation: Optical, Radio Frequency (RF) and Magnetic.

1) Optocoupler: This is probably the most traditional and longest reigning method of sending a drive signal across the isolation barrier. However, optically isolated drive that uses Optocouplers cannot transfer energy so local powering and further gate driving circuit is required. Optocouplers are also highly non-linear and can have long propagation delays. Furthermore, high performance optocouplers can also be expensive.

2) Digital Isolator: A modern replacement to optocouplers. The Digital Isolator uses high frequency RF transmitter and receiver to transmit a signal across the isolation barrier. This is an expensive implementation because it requires relatively complex circuitry, albeit conveniently packaged in an IC.

3) Magnetic Coupling: This approach is very commonly used nowadays. There are two extremes of magnetic coupling implementations:

a) Coreless Transformer: As the operating frequency increases, the required core size decreases and if the frequency is sufficiently high, the core size can approach and become zero and thus yield the Coreless Transformer [1]. This uses a modulation technique, similar to the Digital Isolator, where the low frequency signal is encoded onto a high frequency carrier and everything is conveniently packaged in an IC. However, this method is also costly, and requires local powering.

b) Direct Drive: In this implementation the gate drive signal is directly transferred through gate drive transformer at the power converter driving frequency. The driving frequency can be quite low, e.g. ranging from 40kHz to 150kHz as seen in typical LLC implementations. Low frequency results in a high Volt-Second product, and therefore a relatively large core and a large number of turns are necessary to prevent saturation. This is the lowest cost but the largest implementation. This approach works well for variable frequency drive with fixed 50% duty ratio as required by the LLC converters. However, in typical PWM applications, this aprach can become very large in order to accommodate high duty ratios.

A. Volt-Seconds – the key to optimising magnetic drives

When designing a transformer, one of the first limiting factors that comes to mind, is core saturation. Based on the core material, there is a limitation on the magnetic flux density ΔB which can be calculated by (1).

$$\Delta B = \frac{V \Delta t}{n A_e}$$

$$\begin{gathered} V - voltage\ applied\ to\ the\ input\ winding\ (V) \\ \Delta t - pulse\ width\ (s) \\ n - number\ of\ turns \\ A_e - core\ cross\ section\ area\ (m^2) \end{gathered} \tag{1}$$

$$A_e = \frac{V \Delta t}{n \Delta B} \tag{2}$$

In the interest of minimising the core size, (1) can be re-arranged as (2). The core material, number of turns and operating voltage are going to be fixed by design choice. This leaves only one variable that determines the core size – Δt. In other words, by minimising the Vol-Seconds applied to the transformer we can reduce the required core size.

Given this information, to reduce the size of magnetics required for Direct Drive, the first instinct would be to increase switching frequency. This is not always an option. Oftentimes increasing switching frequency results in reduced converter efficiency due to increased drive power and switching losses in the power switches.

B. The novel approach

The direct drive approach is the lowest cost solution for driving across the isolation barrier. This work introduces a new approach – Magnetic Pulse Drive with the goals outlined below:

- Gate Drive Signal with Energy transfer across the isolation barrier – no local powering.
- Reduced magnetic size compared to Direct Drive approach.
- Implementation volume similar to monolithic approaches.
- Low cost.
- Drive transformer size not dependent on duty ratio or frequency of PWM.

Note: Pulse Width Modulation (PWM) as used in the context of gate driving refers to the variation of the Duty Ratio. The pulse width as described in the context of the new gate drive approach is a separate entity

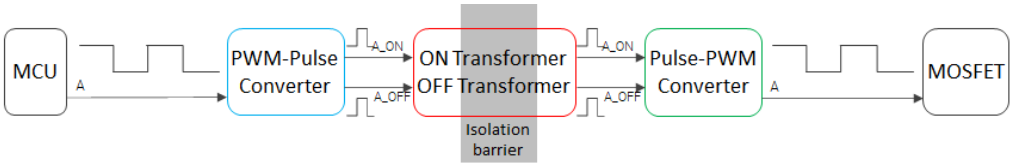

Fig. 1 System diagram of new gate drive approach for a single transistor

II. Magnetic Pulse Drive

The main idea is to decouple magnetic signal and energy transfer from the PWM. This approach can be split into three parts. Fig. 1 shows the system overview diagram. The input is connected to the PWM-pulse converter which then sends ON and OFF pulses through small transformers. These go into Pulse-PWM converter [4] which is fully floating and can drive the power MOSFET directly without any local powering. It is important to point out that this work builds on a proprietary patented technology.

A. Pulse-PWM Converter

This is based on a low-cost IC intended for driving of floating power FETs. The applications range from high-side FETs in half-bridge converters to totem-pole and multilevel converters. The IC itself does not produce any isolation. The application circuit for the purpose of this work is illustrated in Fig. 2. There are two inputs to the IC. One is a voltage pulse indicating the rising edge of the PWM signal, the other is a voltage pulse indicating the falling edge of the PWM signal. R_{ON} + R_{OFF} control the rise time and can be used to reduce V_{GS} while R_{OFF} controls fast turn OFF timing. For this application, an external transistor Q11 is used to augment the turn OFF current carrying capability of the IC70-001. Q11 is exposed to the potential equal to V_{GS} of the power FET. Typically, this means about 10V - 15V so Q11 can be a low voltage N-MOS FET with a V_{DS} rating of about 20V.

It is worth noting that the pulses are not required to be the same width. In fact, the ON pulse is wider because it carries the energy required to turn on the power FET and the OFF pulse can be shorter because there is very little energy required by the circuitry to turn the power FET off.

By design, this gate drive IC has extremely low turn on delay – as seen from the circuit diagram, there is only a diode (D10) and two resistors (R_{ON}, R_{OFF}) between the pulse input and the gate of the power FET. Furthermore, since the pulses to the IC instruct the rising and falling edges, the modulation scheme is not limited by this IC but only by the pattern of pulses arriving to the inputs. A refresh ON pulse can also be sent to keep the power transistor turned on indefinitely, although this feature is not utilised for the application described in this work. The gate voltage is going to be determined by (3).

$$V_{GS} = V_{on\_pulse} - V_{D10} \tag{3}$$

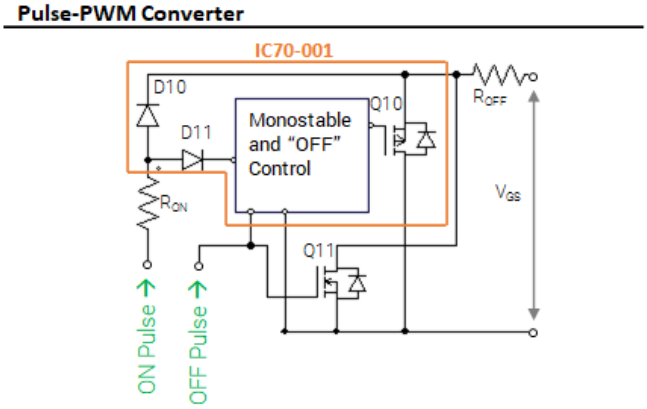

Fig. 2 Pulse-PWM Converter circuit diagram

B. Transformer

The transformer block, as illustrated by Fig. 3, implements two small forward transformers – one for ON and one for OFF pulses. For simplicity, the implementation for both is identical. The input circuit to each transformer is a small, low voltage NMOS transistor (Q1, Q2) with low gate threshold voltage to minimise delays and a freewheeling diode (D1, D2) across each primary winding (L_{pON}, L_{pOFF}) for clamping.

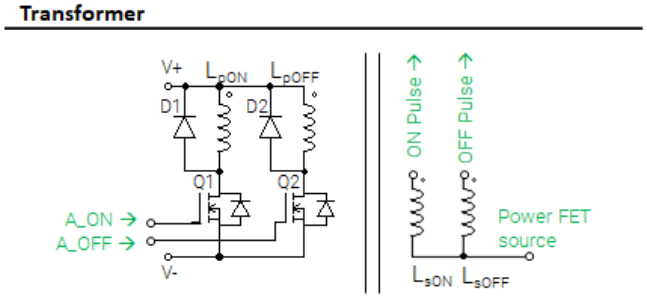

Fig. 3 Transformer circuit diagram

C. PWM-Pulse Converter

Fig. 4 shows the circuit and timing diagram for the PWM-Pulse Converter. This is an edge detector circuit designed to produce a pulse on the rising and falling edges of a PWM signal. The diagram illustrates that the ON and OFF pulses are not of the same width. This is due to delays in the logic ICs. What matters is the ability to control the ON pulse width by tuning values for R and C.

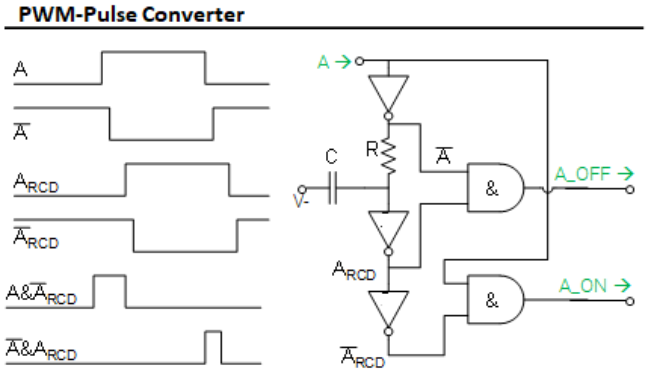

Fig. 4 PWM-Pulse Converter circuit diagram

D. Signal timing overview

Fig. 5 illustrates system signals and points out two delays, d1 and d2 (these are not drawn to scale). Delay d1 is caused by the PWM-Pulse converter as described earlier. Delay d2 is caused by the transformer circuit. All gate drivers have intrinsic delays, and these can be accounted for in the system design.

E. Driving a single transistor

Fig. 6 illustrates the total circuit for the system shown in Fig. 1. The energy required to drive a power MOSFET depends on its input capacitance. The energy transfer in this circuit can be controlled by adjusting the ON pulse width by changing R and C. The combined 'A_ON' and 'A_OFF' pulse width plus PWM deadtime determine the minimum PWM ON time and thus the maximum operating frequency as described by (4). The minimum deadtime is limited by the 'A_OFF' pulse width. This is because while 'A_OFF' pulse is active, the output of the gate driver is essentially short circuited, so any attempt to pump charge in this scenario is a waste of energy. Therefore, we must wait for the 'A_OFF' pulse to expire before sending an 'A_ON' pulse.

$$f_{max} = \frac{1}{(t_{A\_ON} + t_{A\_OFF} + t_{DT}) \times 2} \tag{4}$$

Meanwhile, the minimum operating frequency is determined by power MOSFET V_{GS} leakage current which causes gate voltage to drain over time. This implementation does not send refresh ON pulses and for this reason it is not suitable for keeping a transistor turned on constantly. Also, for applications where varying duty ratio is used to enact control, the minimum and maximum duty is determined by (5) and (7).

$$D_{min} = (t_{A\_ON} + t_{A\_OFF}) \times f_{PWM} \tag{5}$$

$$D_{max} = \frac{1}{f_{PWM}} - (t_{DT} + t_{A\_OFF}) \tag{6}$$

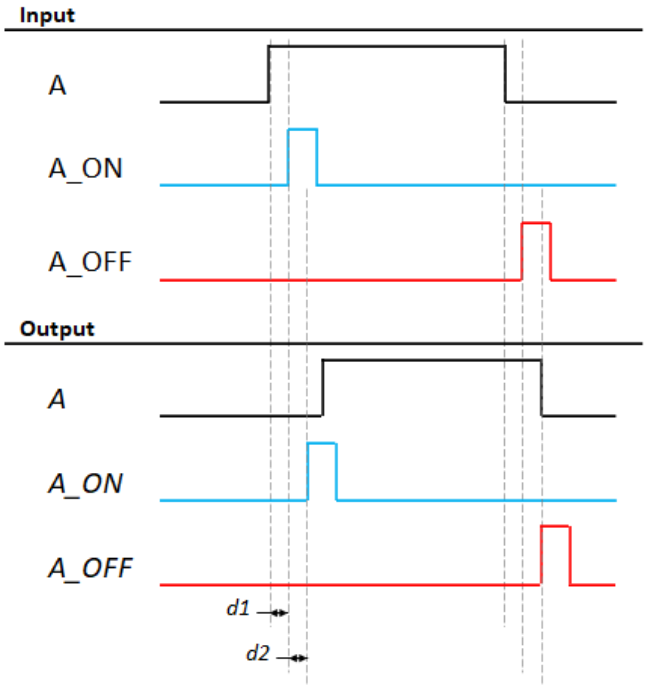

Fig. 5 Input and output signal timing indicating system delays

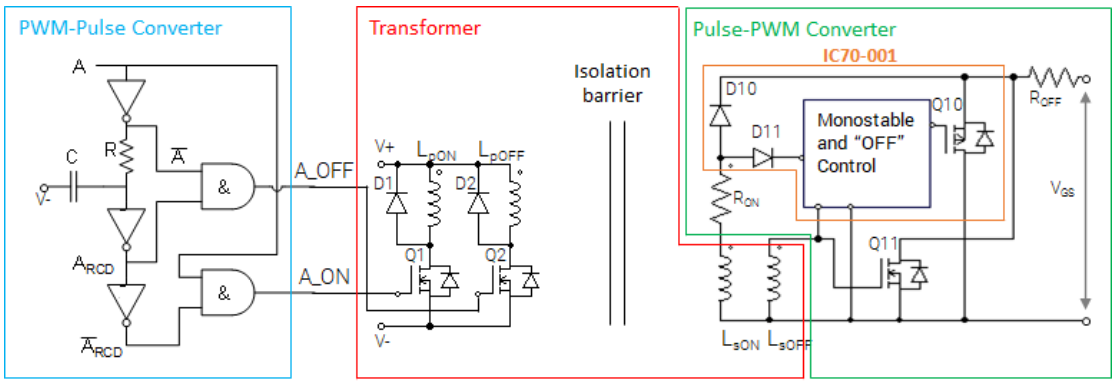

Fig. 6 Circuit overview and operating principal of gate drive approach described in Fig. 1

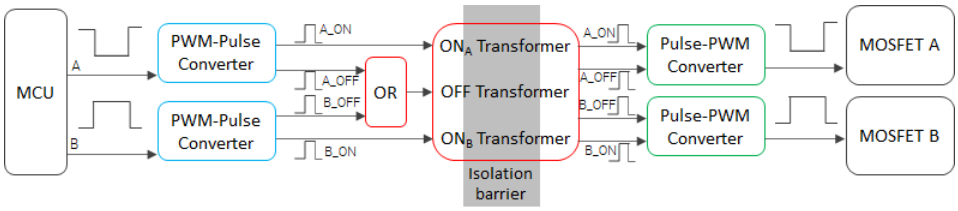

Fig. 7 System diagram of new gate drive approach for a complementary drive

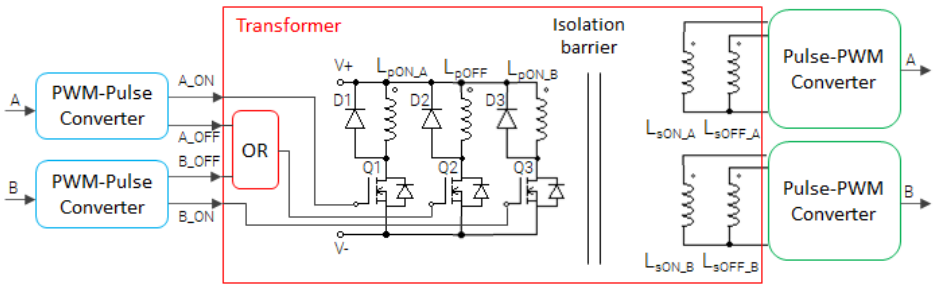

Fig. 8 Transformer circuit for complementary drive

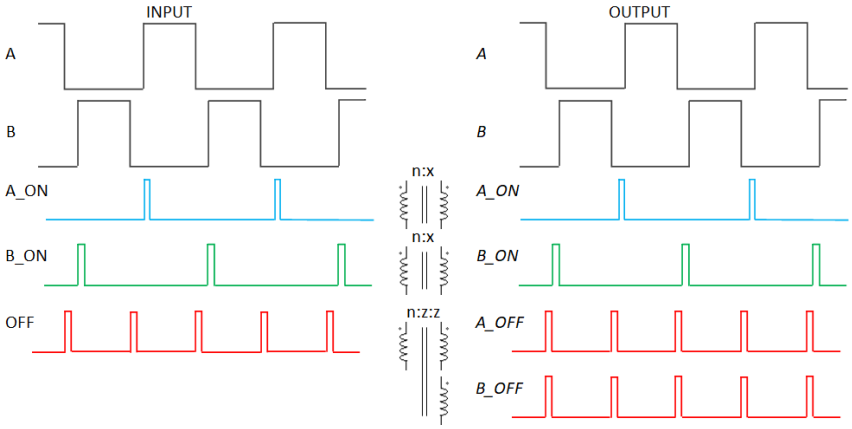

Fig. 9 Showing signals for transformer implementation described in Fig. 8

F. Driving a complementary pair of transistors

In order to add a complementary drive, first instinct would be to simply double up on the implementation, however this would result in a sub-optimum transformer implementation: 4 transformers – two ON and two OFF. Instead, we can combine the OFF pulses into a single transformer. This means that the OFF pulses of phase A and B would be sent to both power transistors together. The new system diagram is shown in Fig. 7. The transformer circuit for the complementary drive is shown in Fig. 8 and the input and output signals are detailed in Fig. 9. It is worth noting that the OFF transformers do not need the same ratio as the turn ON. This is because during turn ON the circuit must send energy but also, must achieve a desired voltage to turn ON the power FET. During turn OFF we simply need to drive small signal devices which takes a lot less energy and operate at much lower voltages. This optimization reduces the size and component count of the transformer implementation by 25%.

III. Design Procedure

There are several limitations that can be imposed on the hardware implementation. This work aims to deliver a practical implementation that is conscious of manufacturing cost and complexity. The design procedure will be illustrated by implementing a complementary drive for a half-bridge LLC converter. In line with keeping costs low, the control and drive card is built on a 4-layer PCB. The transformer windings are implemented in a planar fashion on the PCB. Two layers dedicated to the primary windings and two to the secondary.

A. Transformer ratio

The supply voltage to the control circuit and hence the gate driver is 8V. We want to be driving a 600V SJ FET (Infineon IPW60R170CFD7XKSA1) [7] with a maximum of 12V (any higher is a waste of energy). This gives us maximum transformation ratio of 1.5.

B. Number of turns

The first goal is to fit as many turns as possible in order to reduce ΔB. This number is limited by the fact that we want to achieve galvanic isolation while keeping the size to a minimum while doing it all on a 4-layer PCB.

The winding implementation is done in whole numbers. Given the transformation ratio of 1.5, this yealds the following turn ratios: 2:3, 4:6, 6:9, 8:12, 9:15 and so on.

C. Core choice

The core chosen for this implementation must satisfy multiple requirements. First, the core must have high magnetising inductance, which suggests a material like T38. Second the shape/size has to facilitate implementation for galvanic isolation and be as small as possible. Ideally a custom set of U cores could be designed for this application.

For the purpose of this work, we identified an E8.8 core (TDK B66302G0000X138) [5] and simply removed the middle leg leaving us with a U core as shown in Fig. 10. The useful core metrics are: Cross section area A_e=3.8mm^2 and mean magnetic path length l=26.8mm.

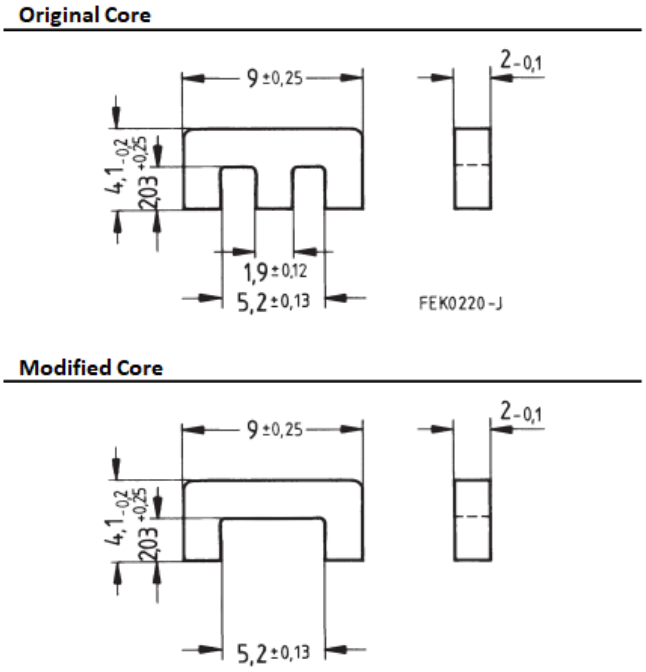

Fig. 10 Original E8.8 core by TDK (B66302G0000X138) (top); Modified core (bottom);

Given the PCB trace spacing of 0.1mm track/gap, the most turns that can be accommodated is 4 per layer, meaning that maximum number of turns for one winding is 8. This leaves us with final turn ratios for the three transformers as follows: A 6:8; B 6:8; OFF 6:4:4. For the ON transformers, given our chosen input voltage of 8V, the ratio of 6:8 will produce 10.6V. The OFF transformers are only driving low voltage circuity that only needs about 5V to work optimally. So, an 8V input with a 6:4 ratio will produce 5.3V.

By using equation (7), we can calculate the expected primary side inductance (the same for all three transformers). Substituting in the values for our core into (8) yields 33.16µH.

$$L = \frac{\mu_0 \mu_e n^2 A_e}{l} \qquad (7)$$

$$\mu_0 - Permeability\ of\ free\ space$$
$$\mu_e - Relative\ permeability$$
$$n - Number\ of\ turns$$
$$A_e - Core\ cross\ section\ area$$
$$l - magnetic\ path\ length$$

$$\frac{1.2566 \times 10^{-6} \times 5170 \times 6^2 \times 3.8 \times 10^{-6}}{0.0268} = 33.16\mu H \qquad (8)$$

D. Transformer implementation

The planar transformer, as implemented on a 4-layer PCB with 0.1mm track/gap, is illustrated in Fig. 11. Cut-outs are shown in green. All winding polarities are done according to the right-hand rule. The input (right) windings are placed on inner layers (2 and 3) providing highest isolation. The output (left) windings are placed on the outer layers (top and bottom) with transformer cores referenced to the output. The silkscreen indicates a 7.5mm gap between input vias and transformer cores. The rest of the isolation relies on the PCB technology.

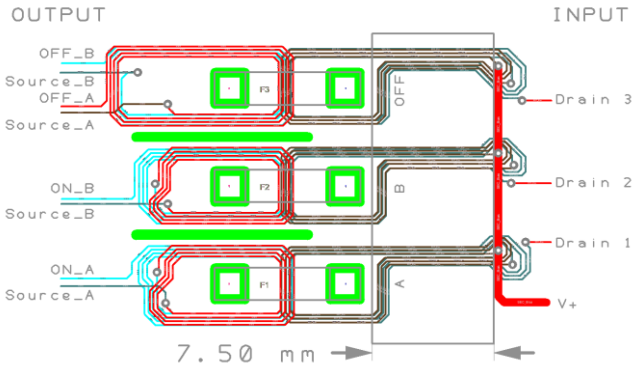

Fig. 11 Transformer PCB implementation

E. Required pulse width

Given that ΔB_{max} for T38 material [6] is ~250mT at 100 °C, by using (9) we can calculate maximum pulse width that will not saturate the transformer. Substituting the values for our design into (10) yields 537.73ns.

$$\frac{\Delta B_{max} n A_e}{V} = \Delta t_{max} \qquad (9)$$

$$\frac{0.25 \times 6 \times 3.8 \times 10^{-6}}{10.6} = 537.73ns \qquad (10)$$

The working principle of this approach is that energy is being transferred while the transformer is ON. This implies that if we want to charge the gate capacitor up to a desired voltage in a chosen amount of time, we need to turn on the transformer for at least that amount of time.

The SJ FET of our choice has a total gate charge Q_g=28nC at V_{GS}=10V. This works out to a gate capacitance of about 2.8nF. Gate resistance, as specified by the datasheet R_G=10Ω. The total turn ON resistance is the sum of R_{ON} + R_{OFF} + R_G. Choosing R_{ON}=6.8Ω and R_{OFF}=3.3Ω gives a total resistance of ~20Ω. By using the time constant τ=RC, we know that voltage on a capacitor will reach 99% after 5τ. Therefore, we can derive (11) for calculating the required pulse width. For 20Ω resistance and 2.8nF capacitance this works out to ~ 280ns.

For the PWM-Pulse converter, C=10nF and R=2.2kΩ, including some circuit delays, give a pulse of about 280ns.

$$t_{ON} = 5R_{total}C_G \qquad (11)$$

F. Maximum circuit currents

Maximum output current I_{o_max} during turn on is given by (12). With our design values, this works out to about 530mA. By using our chosen transformer ratio (6:8), we can work out the maximum input current – I_{in_max} = 398mA. It is important to point out that under normal circumstances, these are only initial current values and the current decreases with time as the gate capacitor is being charged up. A scenario where these currents would be sustained during the full time of the ON pulse, is when the gate driver output is short circuited.

$$I_{o\_max} = \frac{V_{max}}{R_{ON} + R_{OFF} + R_G} \tag{12}$$

IV. Hardware Testing

By following the design procedure outlined above, the gate driver has been implemented as illustrated by Fig. 12. The overall implementation takes up an area of ~715mm^2 with all SMD components mounted on the top side. It is important to note that ~140mm^2 (~20%) of this is dedicated to the isolation barrier.

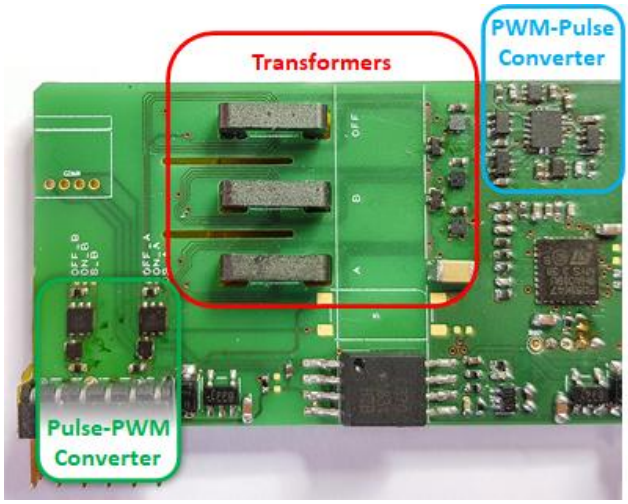

Fig. 12 Proposed Complementary Gate Driver implemented on a 4-layer PCB

The circuit components are listed in TABLE I. Estimating implementation cost for this prototype would not be fair because most of the input circuitry should ideally be integrated into a single IC. This would cut the cost, complexity and size down significantly. Keeping in mind that this approach does not require local powering and the simple circuit is made of a few logic gates and small signal transistors. The overall cost is expected to be below $1 for driving a complementary pair of SJ FETs across the isolation barrier.

TABLE I. Complementary Gate Driver Bill of Materials

Component	***Description***	***Count***
INVERTER	(single) SN74LVC1G14DRLR (TI)	2
INVERTER	(dual) 74LVC2G14,125 (NEXPERIA)	2
AND gate	(quad) 74AHC08BQ,115 (NEXPERIA)	1
OR gate	(single) 74LVC1G32GW,125 (NEXPERIA)	1
R	2.2k 1005M 1%	2
C	100pF 5V 1005M	2
R_{ON}	6.8R 1005M 1%	2
R_{OFF}	3.3R 1005M 1%	2
D1/D2/D3	BAV70T,115 (NXP)	2
Q1/Q2/Q3	NTA4153NT1G (ON Semiconductor)	3
R_{Q1}/ R_{Q2}/ R_{Q3}	Gate pull-down 47k 1005M 1%	3
U8.8	Modified B66302G0000X138 (TDK)	6
Q11/Q12	DMN2400UFD (DIODES Inc)	2
IC70-001	Gate Drive IC70-001 (ICERGi)	2
PCB	4-Layer (part of control card)	*

A. Performance waveforms

Fig. 13 shows the gate driver end-end turn on delay and gate voltage rise time. The rise time can be adjusted by tuning R_{ON} + R_{OFF}. Fig. 14 shows end-end turn off delay and gate voltage fall time. The fall time can be adjusted by tuning R_{OFF}. Fig. 15 and Fig. 16 show input pulses, (created by the PWM-Pulse converter) driving a complementary pair of SJ FETs. It is also worth noting the minimum PWM deadtime illustrated by Fig. 16. The deadtime can be reduced further by reducing the 'OFF' pulse width, however in this PWM-Pulse converter it is not adjustable. It is also possible to skip the PWM-Pulse converter and produce pulses of desired width directly from the microcontroller.

Fig. 17 illustrates the delays described by Fig. 5. Delay d1 is caused by the first inverter in the PWM-Pulse converter (diagram in Fig. 4) and delay d2 is caused by the transformer circuit (diagram in Fig. 3). Delay d2 can be minimised by selecting a faster MOSFET (Q1, Q2, Q3) with a low turn on threshold voltage.

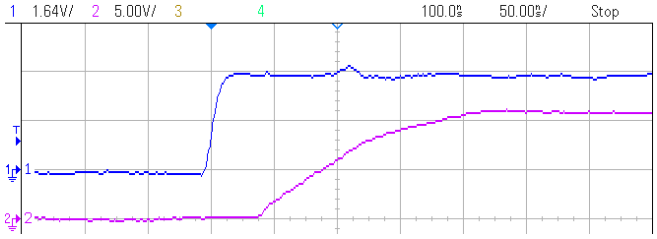

Fig. 13 Turn on transition while driving SJ FET with new gate driver. Input (BLUE), Output (PURPLE).

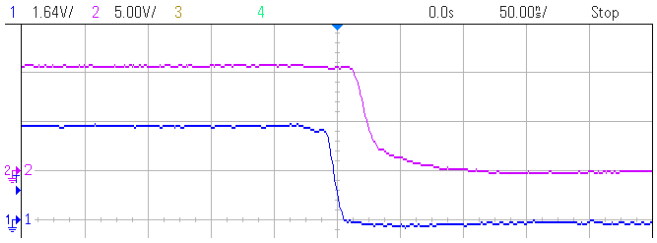

Fig. 14 Turn off transition while driving SJ FET with new gate driver. Input (BLUE), Output (PURPLE).

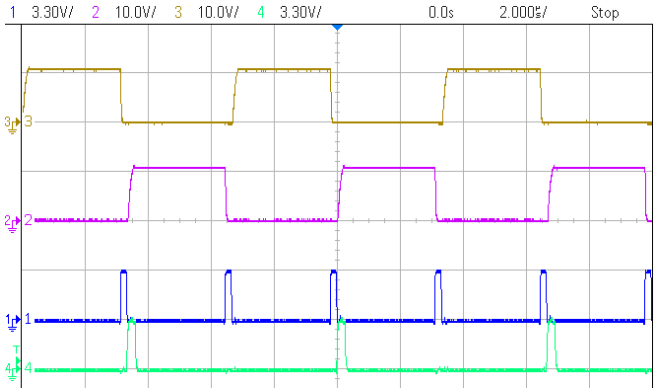

Fig. 15 Driving a complementary pair of SJ FETs with new gate driver. Gate A (PURPLE), Gate B (GOLD), 'OFF' pulse (BLUE), 'A_ON' pulse (GREEN).

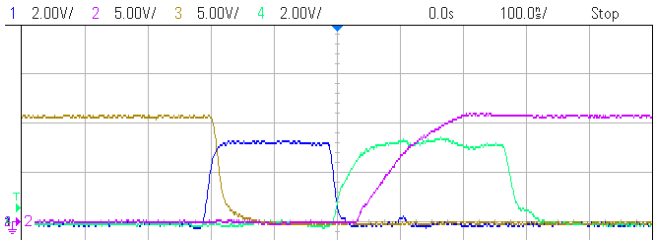

Fig. 16 Zoom in on detail show in Fig. 15.

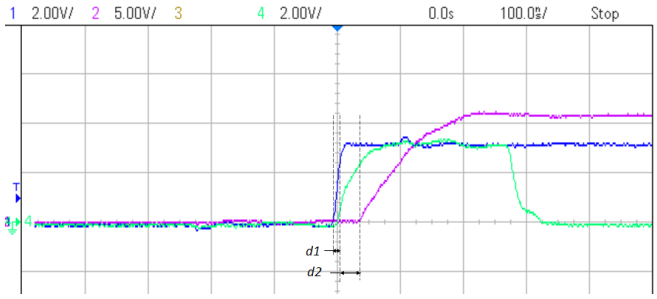

Fig. 17 Showing signal delays described in Fig. 5. 'A' (BLUE), 'A_ON' (GREEN), '*A*' (PURPLE).

B. LLC Converter Using New Gate Driver

The proposed gate driver with exact values and implementation as described in sections III and IV has been used to drive a half-bridge split-capacitor LLC converter as part of a prototype end-end AC-DC power supply which is illustrated in Fig. 18. The unit is rated for 1kW 12V with no power derating from $230V_{ac}$ down to $115V_{ac}$ and has a power density of $25.6W/in^3$. The designed holdup time is 10ms and it qualifies for Titanium efficiency rating as shown in Fig. 19. LLC efficiency is shown in Fig. 20.

Fig. 18 1kW 12V AC-DC Power Supply 200mm x 80mm x 1U

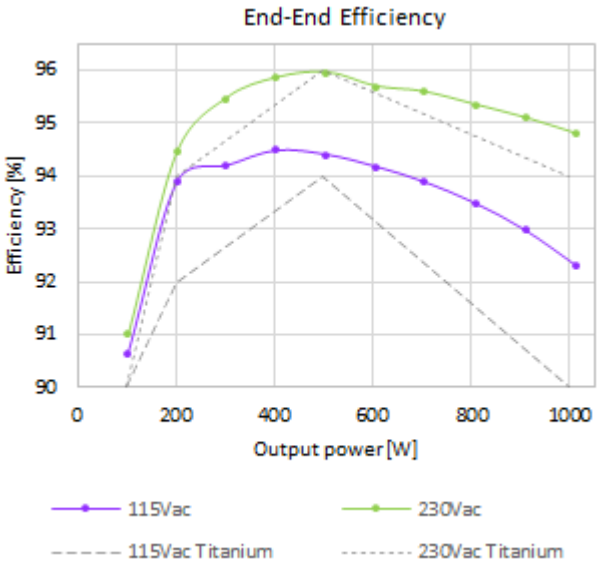

Fig. 19 1kW 12V AC-DC End-End efficiency

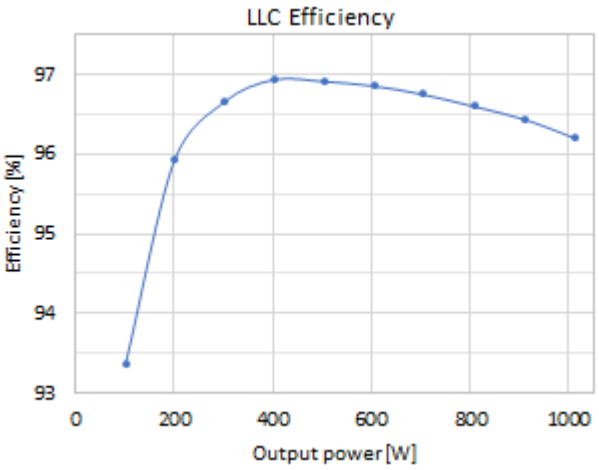

Fig. 20 1kW 12V LLC Efficiency using new half-bridge driver

V. Conclusion

A novel gate driving approach has been introduced in this paper. Two significant cost-cutting advantages are that this gate driver does not require local powering and it consists of low intrinsic cost circuitry. This implementation is aimed at driving half-bridge topologies from the secondary side, with specific focus on galvanic isolation, manufacturing cost and space requirements. An illustrative design procedure outlines the steps for an example LLC application; however, this approach has wide applications including totem-pole PFC and multilevel converters [2]. Furthermore, the implementation of the pulse transformers can be much more compact when only functional isolation is required, and the input circuit can be reduced to an IC for maximum cost and space savings.

VI. References

[1] S. Y. Hui, Henry Shu-Hung Chung and S. C. Tang, "Coreless printed circuit board (PCB) transformers for power MOSFET/IGBT gate drive circuits," in IEEE Transactions on Power Electronics, vol. 14, no. 3, pp. 422-430, May 1999, doi: 10.1109/63.761685.

[2] T. T. Vu and E. Mickus, "99% Efficiency 3-Level Bridgeless Totem-pole PFC Implementation with Low-voltage Silicon at Low Cost," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 2077-2083, doi: 10.1109/APEC.2019.8721928.

[3] R. Liu and C. Q. Lee, "Analysis and design of LLC-type series resonant convertor," in Electronics Letters, vol. 24, no. 24, pp. 1517-1519, 24 Nov. 1988, doi: 10.1049/el:19881036.

[4] G. Young, “Gate drive circuit for a semiconductor switch”, U.S. Patent 9 590 621 B2, Mar. 2017.

[5] TDK, “E 8.8 Core and Accessories”, https://www.tdk-electronics.tdk.com/inf/80/db/fer/e_8_8.pdf, accessed on 2021-02-10

[6] TDK, “SIFERRIT material T38”, https://www.tdk-electronics.tdk.com/download/528868/a1b2c78870f91bc39bb4d281dba6b50c/pdf-t38.pdf, accessed on 2021-02-10

[7] Infineon, “600V CoolMOS^a CFD7 Power Transistor”, https://www.infineon.com/dgdl/Infineon-IPW60R170CFD7-DS-v02_01-EN.pdf?fileId=5546d4625e763904015ea46190b731e6, accessed on 2021-02-17

[8] Infineon, “800W Platinum server power supply”, https://www.infineon.com/dgdl/Infineon-ApplicationNote_EVAL_800W_PSU_4P_C7-AN-v01_00-EN.pdf?fileId=5546d4625cc9456a015d36354c482b7a, accessed on 2021-02-17