The ICERGi, Low-cost Bridgeless Totem-pole PFC Platform Delivers 99% Efficiency at 100 Watts/in^3

It is overlooked in recent literature that high efficiency, above 99%, for PFC front-end stages can be achieved by a bridgeless totem-pole topology and MOSFET devices. This approach offers lower cost and design risk than using WBG devices. Design concerns revolving around the cost of WBG devices, the non-standardized packaging, and bulky magnetics led ICERGi to develop a lower-cost and compact platform with enhanced system efficiency. This article discusses a compact, yet highly efficient PFC platform, using 150V MOSFETs for the bridgeless totem pole topology enabled by ICERGi ARM Cortex M0 control and its driver technology.

1. Bridgeless Totem Pole for Highest Efficiency

In offline switched mode AC/DC power supplies, active power factor correction (PFC) is generally required for input power exceeding 75W, as mandated by IEC 61000-3-2 [1]. The purpose of the PFC is to program the input current of the power supply to follow the wave shape of the AC mains voltage. This has been historically achieved by low-cost diode full-bridge rectification and a single-switch boost converter at the expense of low efficiency and bulky designs.

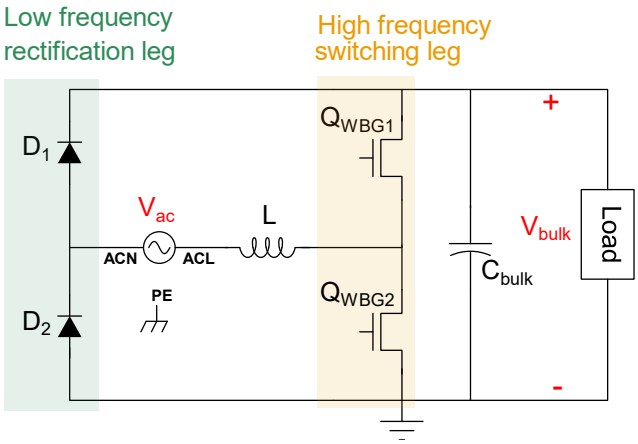


Figure 1: Conventional bridgeless totem-pole PFC with diode rectification

The bridgeless totem pole topology as shown in *Figure 1* has been used recently to achieve the highest efficiency for the PFC. The idea is to reduce conduction loss and consequently increase circa 1% efficiency gain at low line by replacing diode full-bridge rectification with half-bridge rectification. Conduction loss in the boost stage is also lower because the switching leg consists of active devices only. The efficiency can be further enhanced by using high voltage Super Junction (SJ) MOSFETs for the low frequency rectification leg. Such an implementation may also enable bidirectional power transfer which is relevant to self-consumption and EV applications.

The conventional totem-pole PFC as shown in Figure 1 faces several practical challenges due to the hard switching of the high frequency leg. Using standard Super Junction 600V MOSFETs is immediately ruled out because of their excessive reverse recovery loss. This leads to

the exploration of Wide-Bandgap (WBG) devices, e.g. GaN, SiC, in recent applications [2], [3]. However, for designers, these WBG devices are currently not standardized making second source challenging, and are high cost. What is often overlooked is the impact on the magnetic components of using WBG devices. In particular, the hard-switching loss confines the operating frequency of WBG devices to less than 100kHz, which results in a high volt-seconds product being applied across the inductor. This indicates that the WBG implementation does not provide any benefit of magnetics size reduction as compared to the conventional PFC solution. Additionally, the volt-second product indicates how much differential EMI noise will be generated by the PFC stage. Low volt-seconds product is always desired and is delivered in the ICERGi platform (down 75%).

ICERGi has developed enabling technology for a bidirectional platform which addresses the major challenges associated with the existing WBG-based implementation focusing on low cost driver and control technology. These developments deliver:

- Use of standard MOS switches with multiple second sourcing at low cost.
- Driver technology that is compact, isolated
- Control technology and fully developed algorithms based on an off-the-shelf, ARM Cortex M0 device.
- 4x lower volt-seconds stress on the main PFC inductor reducing volume, EMI and losses.

2. ICERGi 3-Level Implementation for Lower Cost, Compact, and Lower Design Risk

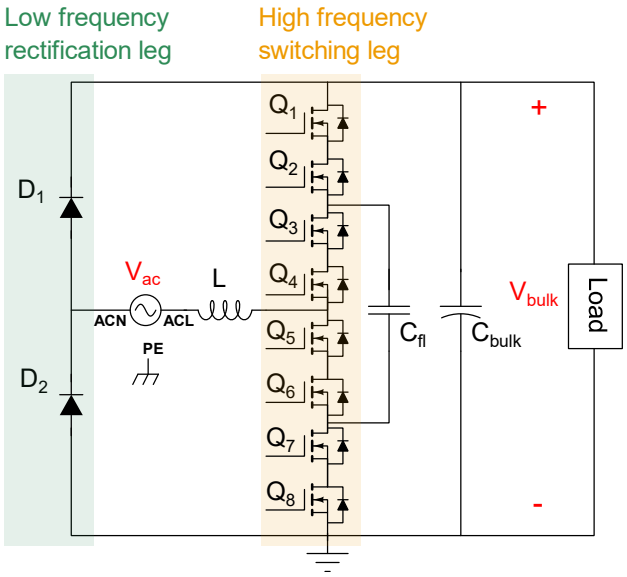


Figure 2: 3-Level bridgeless totem-pole PFC with diode rectification

Given the fact that the reverse recovery issues are more relevant to 600V MOSFETs than to 150V counterparts, the hard switching challenges associated with the bridgeless totem pole PFC can be elegantly addressed by exploiting multilevel conversion [4]. In particular, the 2-level high frequency switching leg can be replaced by a 3-level flying capacitor switching leg as illustrated in *Figure 2*.

The 3-level switching leg operates with phase cancellation, resulting in reduced voltage applied to the PFC inductor for reduced time [9]. This innovation enables a 4 x reduction in volt-seconds product and 2 x reduction in operating voltage of switching devices. Those features can be translated into:

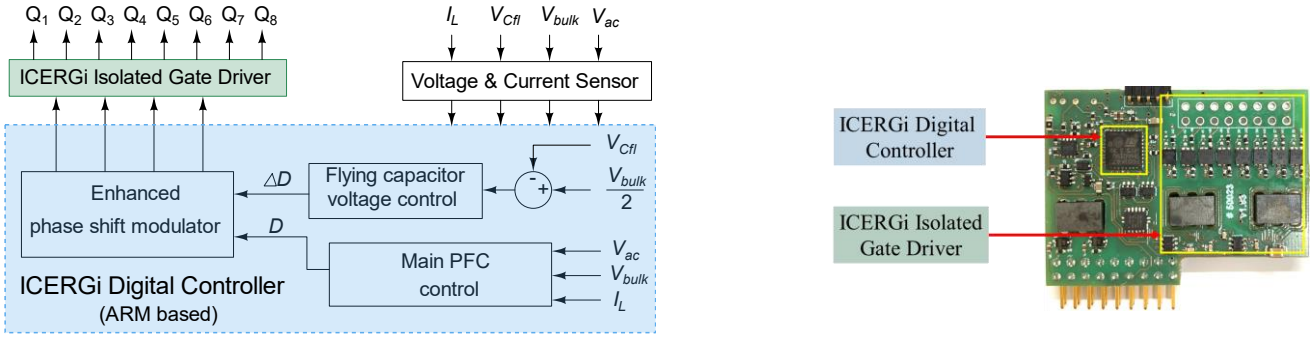
- 4 x lower differential EMI noise.
- A 4 x smaller PFC inductor and smaller EMI filters.
- Enabling the use of 300V Silicon switching devices instead of 600V GaN/SiC FETs. For performance and cost optimization, a 300V-rating composite switch can be implemented by connecting 2 x 150V MOSFETs in series. This explains the reason for 8 x 150V MOSFETs deployed in *Figure 2*. Voltage sharing between series connected MOSFETs can be achieved by using hybrid clamping control and gate drivers with precise delay matching [5], [7].
- Inherently lower dV/dt and dI/dt which is of value in limiting EMI/EMC effects.
- Improved low-line efficiency

3. Versatile Hardware Platform

A. Control and Drive

The ICERGi PFC has been implemented as a scalable and mappable hardware platform that can be deployed for a wide range of applications. This is achieved by exploiting the benefits of digital control and low-cost isolated gate drive approaches as discussed in [5].

A control and drive solution with enhanced phase shift modulation is illustrated in Figure 3(a). A detailed description of the control scheme for ARM Cortex M0 implementation followed by ICERGi's low cost Isolated driver technology is presented in [7]. The isolated gate drive circuits deliver both PWM control signals and energy to the gates of 150V MOSFETs, removing the need for a bias supply.



(a) Block diagram of ICERGi digital control & drive solution *(b) Hardware implementation*

Figure 3: Integrated drive and control card designed for multiple deployments of the 3-level totem-pole PFC

The control architecture as implemented in Figure 3(a) offers significant flexibility in product development. In particular, the main PFC control block can be updated with different algorithms for different deployments. This point is further explored in [6].

The ICERGi drive technology enables the driving of multiple switching devices with low component counts at low cost by obviating the need for local power supplies as typically required by commercial isolated driver ICs. This self-powering feature enables compact implementation of the proposed drive and control architecture. In particular, the ARM Cortex M0-based digital controller and 8 isolated drivers can be easily housed in a compact low-cost daughter board as demonstrated by Figure 3(b). Here, the driver technology provides 8 isolated drive channels in 625mm^2 (78mm^2/channel) of board space. The magnetic elements are planar E-cores. Since the energy to switch is derived from the drive signal, the need for a bias supply is removed leading to significant design simplification. The digital controller can be used in various deployments when flashed with different set of firmware for different end applications. PFC and grid-tied Inverter have been

implemented to date. This approach has allowed the inherent advantages of multilevel technologies to be realised in a practical and cost-effective fashion at relevant power levels, i.e. 600W-3kW range as needed for most of the single-phase AC/DC and DC/AC marketplace.

B. Power Stage Design

It will be recognized that the circuit diagram as depicted in *Figure 2* has been simplified for ease of presenting and understanding. The following circuits must be included to achieve reliable operation of the design in practice.

- Inrush current during start-up can be managed by an NTC thermistor and a relay. Inrush diodes are also required to provide an alternative low impedance path to the bulk capacitor C_{bulk}.
- Flying capacitor Cfl is pre-charged before MOSFETs start switching. The digital PFC controller monitors and regulates the flying capacitor voltage at start-up and during normal operation [7].
- Conducted EMI noise generated by the PFC stage is designed to comply with the class B limits as specified by IEC 61000-3-2. Therefore, two-stage filtering is implemented at the input of the converter as illustrated in *Figure 4*.

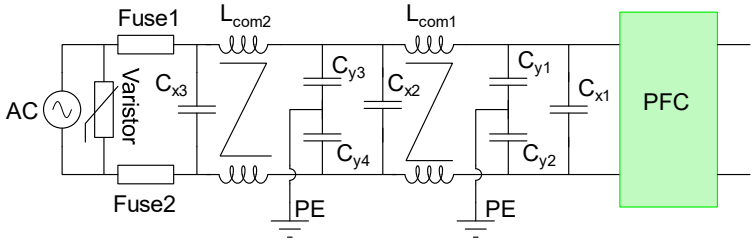


Figure 4: Two-stage EMI filter with dual fusing and a varistor for differential mode surge protection. Additional varistors may be required for common-mode surge protection depending on applications

A PFC platform meets specifications as listed in Table 1. One application is the front-end stage of a 1kW universal AC/DC power supply significantly enhancing low line efficiency and attendant low line derating specifications. The analytical procedure as documented in [8] provides a practical engineering tool to design components for the power stage. Summarized in Table 2. are the major hardware components including a 2-stage EMI filter and a 5W bias supply.

Table 1: 3-level PFC design specifications for universal input 12A applications

Universal line voltage, V_{ac}	$85V_{ac}$ – $265V_{ac}$
Line frequency f_{ac}	50Hz
Nominal output voltage, V_{bulk_nom}	$400V_{dc}$
Switching frequency, f_{pwm}	66kHz
Maximal continuous output power, P_{out_max}	2.4kW @ 230Vac 1.3kW @ 115Vac
Maximal continuous input current I_{ac_max}	12Arms
Efficiency η_{min} Highline 50% load (1200W) Lowline 50% load (600W)	98.5% 97.3%
Maximal pk-pk doule-line frequency output voltage ripple ΔV_{bulk}	40V
Maximal pk-pk flying capacitor voltage ripple ΔV_{fl}	20V
Maximal pk-pk inductor current ripple ΔI_L	3.2A

Table 2: Power stage build of material (BOM)

Main inductor L= 500uH	1 x 60u permeability Sendust core, 72 turns of 1mm diamter enamelled wire
Bulk capacitor C_{bulk}	2 x 330uF 450V Electrolytic
Flying capacitor C_{fl}	5.4uF 450V Film // 440nF 450V Ceramic
Switching leg	8 x 150V 16mR MOSFET BSC160N15NS5 in 5mm x 6mm package
Rectification leg	15A 800V Diode Bridge GBU15K-BP
EMI filter	3 x 1uF 310Vac X- capacitor 2 x 4.4mH common mode choke 4 x 470pF 310Vac Y- capacitor
Bias supply	5W quasi-resonant flyback converter

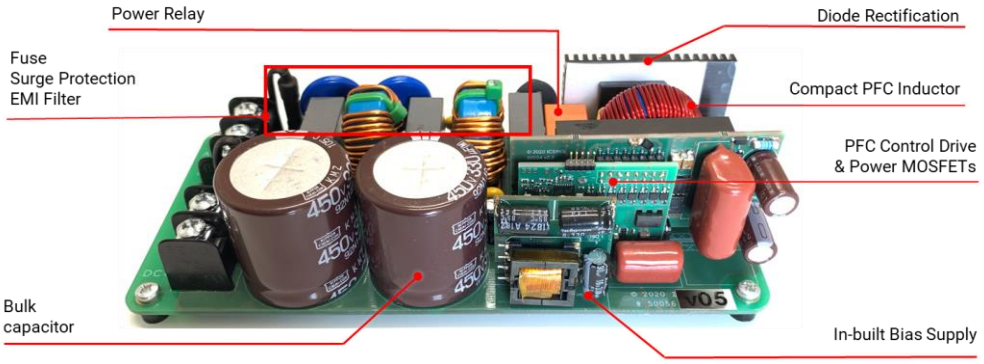
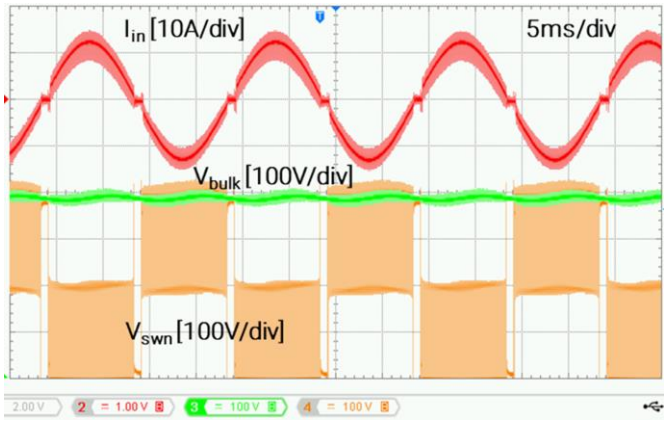


Figure 5: Universal input 12A PFC demonstrator IC3LPFC-12A with compact inductor and EMI filters. The whole design is comfortably fit in a small footprint of 72mm x 158mm x 38mm

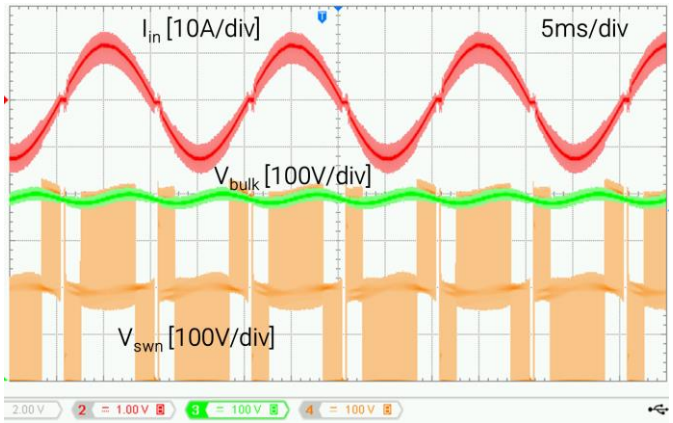
C. Performance Data

Voltage and current waveforms captured at 230Vac and 115Vac with resistive load are presented in *Figure 6*. The switched node voltage shows steps of 200V which is well within the aggregate voltage rating of two series-connected MOSFETs. *Figure 6* also confirms that the converter operates in a stable manner with no sign of voltage imbalance. The current waveform shows minimal distortion, suggesting high power factor values and low total harmonic distortion (THD).

Figure 7 presents the PFC stage efficiency and total losses measured at both high line and low line with a 100W step load. The stage efficiency peaks around 98.8% at 230Vac and 97.5% at 115Vac. The peak efficiency at 230Vac can be lifted to 99% by replacing the diode rectification with high voltage SuperJunction MOSFETs but this implementation may increase the design BOM cost by 30% to 40%. The efficiency curve is relatively flat and shows modest roll-off at full power.

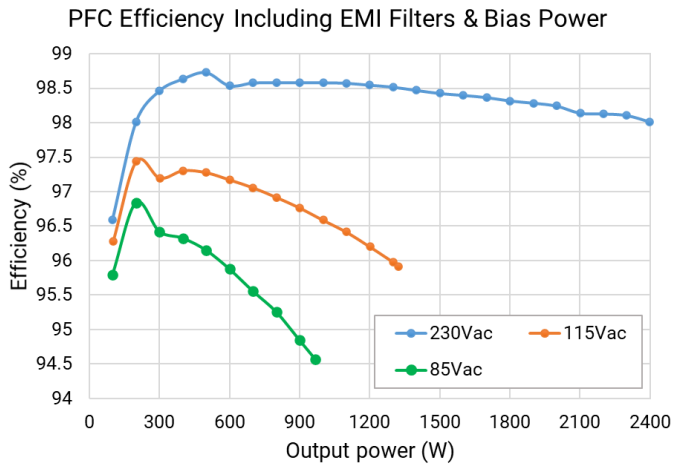


(a) Low line (115Vac) and 1kW resistive load



(a) High line (230Vac) and 2kW resistive load

Figure 6: Operational waveform of the 3-level totem-pole PFC at low line and high line



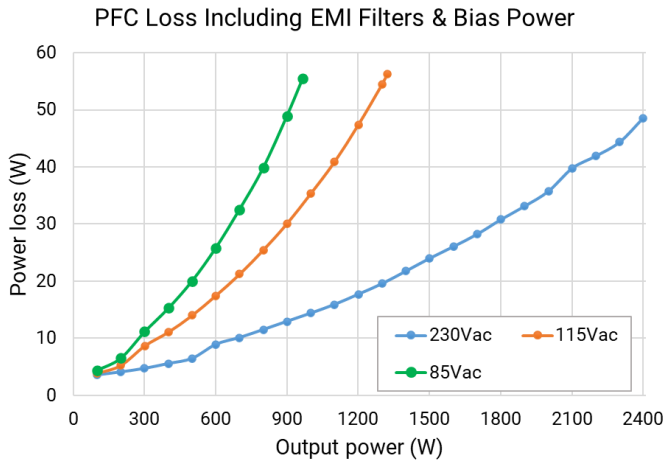
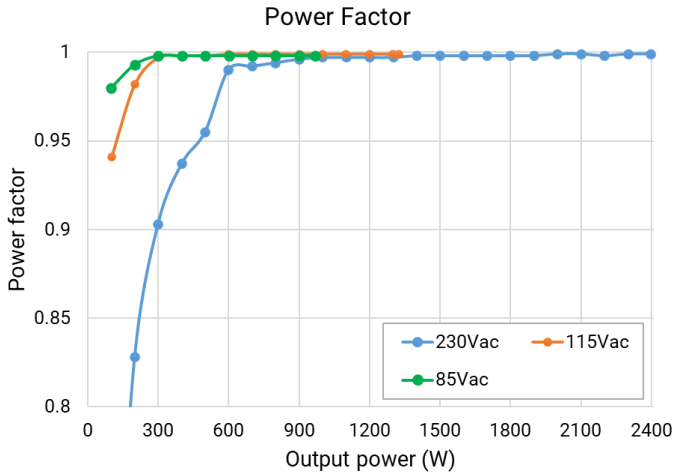


Figure 7: Efficiency and total power loss of the 3-level totem-pole PFC designed for universal input 12A applications



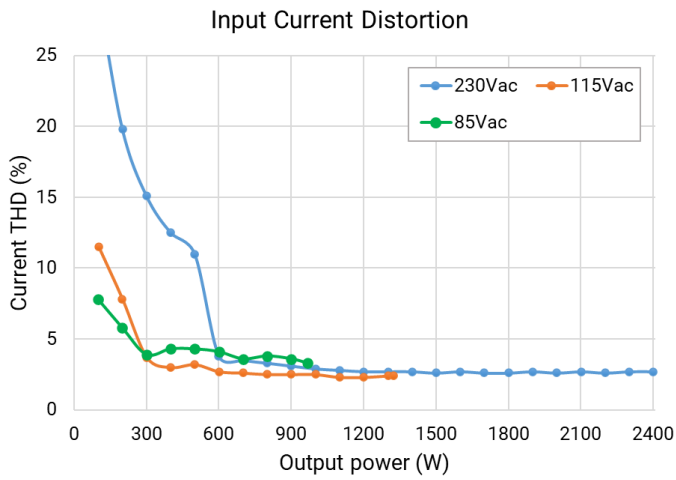


Figure 8: Power factor and current THD of the 3-level bridgeless totem-pole PFC

The digital PFC controller has a current loop that is designed to dynamically adapt its gain depending on the PFC inductance value. This maximizes the control bandwidth without compromising system stability. The outcome is high power factor, i.e. above 0.99, and low current distortion, i.e. below 5%, for 600W-2.4kW load as demonstrated in *Figure 8*.

4. Summary

The ICERGi low-cost high efficiency PFC platform using the 3-level bridgeless totem pole topology and 150V MOSFETs provides industry leading efficiency with diode rectification. This efficiency can be further enhanced by using line synchronous rectification [5].

The document confirms that established low-cost silicon can achieve better than 99% efficiency in CCM totem-pole PFC rectifiers as generally associated with WBG devices. Multilevel solutions also have sustainable competitive advantage in magnetics size (four-times reduction), EMI/EMC performance, as well as an expected long-term cost advantage over conventional (2-level) WBG (SiC and GaN) -based implementation through second sourcing opportunities of switches, lower cost driver technology, smaller magnetics, and reduced bias supply requirements.

The control and driver technology may be licenced with a variety of delivery models for the controller firmware and driver technology devices.

References

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[8] ICERGi, “2.4kW 12A PFC Power Stage Design and Loss Analysis”, Application Note AN010

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