Stacked Multi-Phase ("SMP") Approaches for Power Factor Correction

1. Backdrop

Power Factor Correction is a very common requirement in ACDC power conversion. Typically, at input powers exceeding 75W in general-deployment ACDC power conversion – and at lower power levels for lighting applications – this requirement becomes relevant. Either the power factor needs to exceed a value of 0.9 over some part of the load range, line current harmonics need to meet requirements, or both. IEC61000-3-2 is the principal Standards document in this context.

2. Power Factor Correction ("PFC") Implementation

PFC can be implemented using a wide variety of architectures and topologies. The most common approach involves usage of a boost converter to convert the input AC voltage (usually the "universal line" voltage range from 90V RMS to 264V RMS, 47Hz-63Hz) to a nominal DC level of 400V.

This approach is relatively straightforward and has become the industry standard. The boost converter stage supplies a quasi-constant voltage which is conducive to obtaining high efficiency in downstream stages. The 400V operating range has led to wide availability of standard electrolytic capacitors with 400V-450V rating, and the energy density of such capacitors is materially higher than is available for example at voltages of 100V or below.

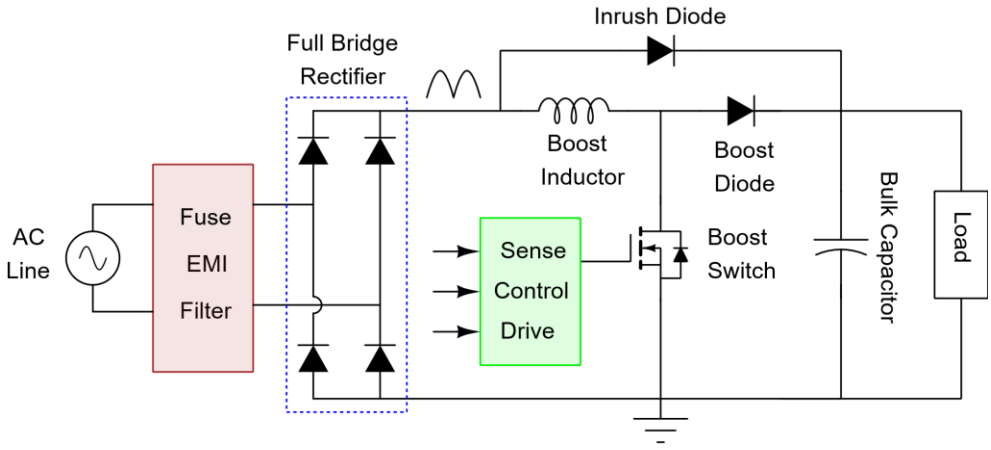

Figure 1 – Showing Boost Power Factor Correction Stage

So – the goal is to retain all these favourable characteristics, allow usage with standard capacitor values and "downstream" stages, and enhance performance.

And performance enhancement is possible in terms of efficiency and in terms of minimising requirements on passive components.

3. Improving PFC Performance – “Bridgeless” Approaches

The ICERGi goal is to reduce losses in power factor correction by 50% as compared with “classic” designs as in Figure 1, with corresponding savings in volume, and at comparable cost. Peak efficiency in “classic” power factor correction stages, including input EMI filtering and rectification, is typically between 94% and 97% - and hence a goal of achieving figures in the range of 97%-98.5%, with particular importance attached to getting high efficiency at the usual constraint condition of low-line operation. Halving power loss has immediate benefits in simplifying thermal design and/or allowing more compact construction – and longer-term gains in terms of energy saving, with a direct cost saving and the benefits of compatibility with best “green” practice and standards.

A totem-pole structure has been widely used as a technique for reducing conduction loss – and is one of a family of converter types termed “bridgeless”. In the classic “single ended” PFC approach as in Figure 1 the input current at any given time will flow through two diodes in the rectifier bridge and through either an active switch or diode within the boost stage. The totem-pole structure as in Figure 2 requires just two semiconductor devices to be conducting at any given time. Losing conduction losses associated with a diode voltage drop in the bridge rectifier typically translates at low line into approximately 0.8% efficiency gain – usually seen as valuable but not in itself promoting wide usage of bridgeless designs.

The totem-pole approach of Figure 2 also is seriously challenged in terms of usage of Si MOSFETs types currently optimised for low-Rdson – with devices of the 600V-650V type usually exhibiting relatively slow switching and very poor reverse recovery performance. Some improvement in reverse recovery performance is possible with “fast diode” types, but with reduced availability and compromise in Rdson values. Alternatively, composite devices can be constructed, so as to obviate the reverse-recovery challenge.

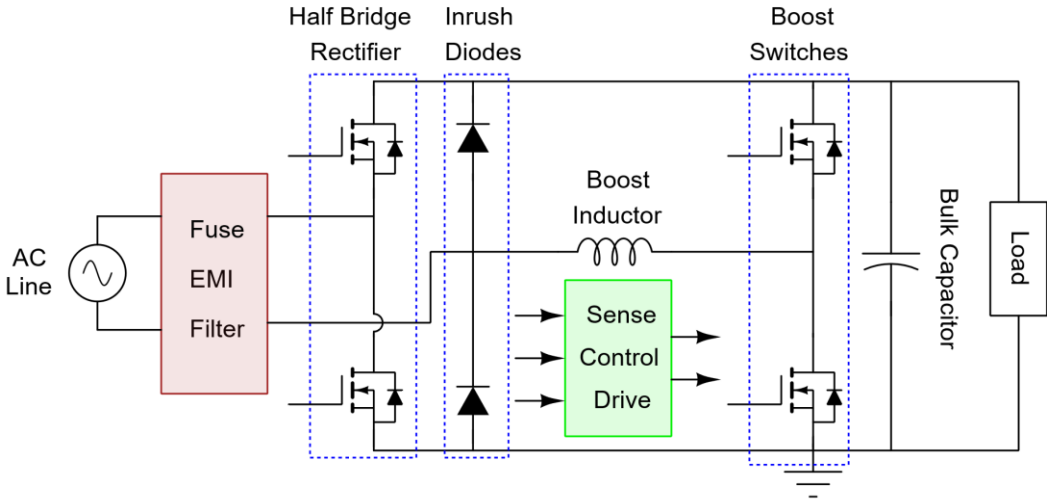

Figure 2 – “Totem Pole” Boost PFC Stage

Totem pole structures of such types appear as ideal candidates for GaN FET deployment, and successful usage of such devices has been widely reported. There remains however the issue of high volt-seconds applied across the inductor and the operating frequency may well be constrained by the parasitic capacitances getting switched at 400V.

One can thus look further in terms of opportunities to optimise performance.

4. Stacked Multi-Phase Approaches

Multilevel inverter legs have been used for some time in higher power, higher voltage deployments, where the available rating of semiconductor switches has typically been below the operating voltage.

The advantages of multilevel converters are well established – including the ability to operate each “sub-stage” or “cell” at a relatively low frequency with lower-voltage devices – and have greatly reduced ripple (and at higher frequency) present in the inductor.

Deploying these technologies at power levels associated with volume single-phase ACDC conversion markets – perhaps in the range 300W-3kW – has required development of effective but low-cost balance-enforcement circuitry, new control implementations and algorithms, and effective and precise low-cost gate drives.

ICERGi designs incorporate these approaches in multilevel “Stacked Multi-Phase” legs that can be incorporated into totem-pole structures, as shown in Figure 3.

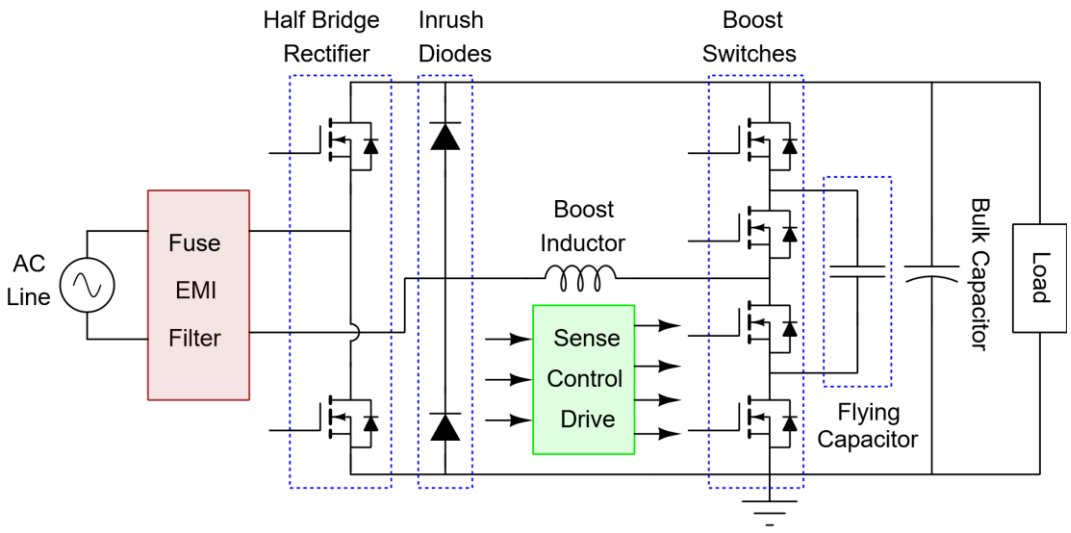

Figure 3 – Showing ICERGi multilevel “Stacked Multi-Phase” leg incorporated into totem-pole structure

The key advantages of these approaches, and that allow them approach cost-parity, are:

- Low volt-seconds applied to the input inductor as shown in Figure 4 – resulting in a lower value of required inductance for given ripple, thus yielding a smaller inductor and the opportunity to design a materially smaller EMI filter. Figure 5 implies low conducted-EMI noise nature of multilevel power conversion.
- Each switching stage can use 150V, 200V or 250V FETs depending on the level count and overall voltage rating needed. Precision drive allows commutation with minimal loss due to low applied voltage and due to the good switching characteristics of devices in this voltage rating class. Fully synchronous operation and availability of devices with low Rdson and excellent figure of merit (FOM) reduce conduction and drive losses.
- Low heat dissipation in each FET, given the distributed nature of heat generation, allows standard low-cost surface-mount techniques to be used, with Bond-Ply™ or Gap-Pad™-type material readily used to provide the limited amount of thermal transfer to heat spreader elements as may be required.

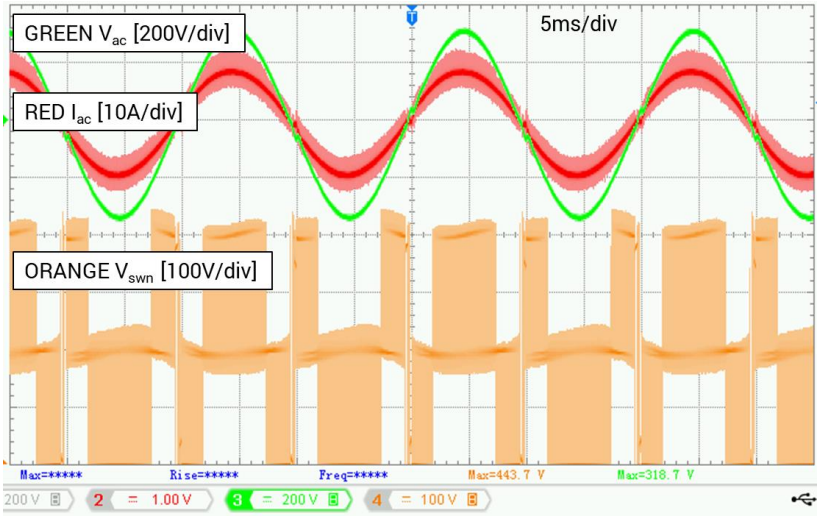

Figure 4 – Showing operational waveforms of the 3-level totem-pole PFC at 230Vac and 1.5kW. The switched node voltage in orange confirms that the inductor experiences significant lower volt-seconds as compared to that of a conventional (2 -level) PFC.

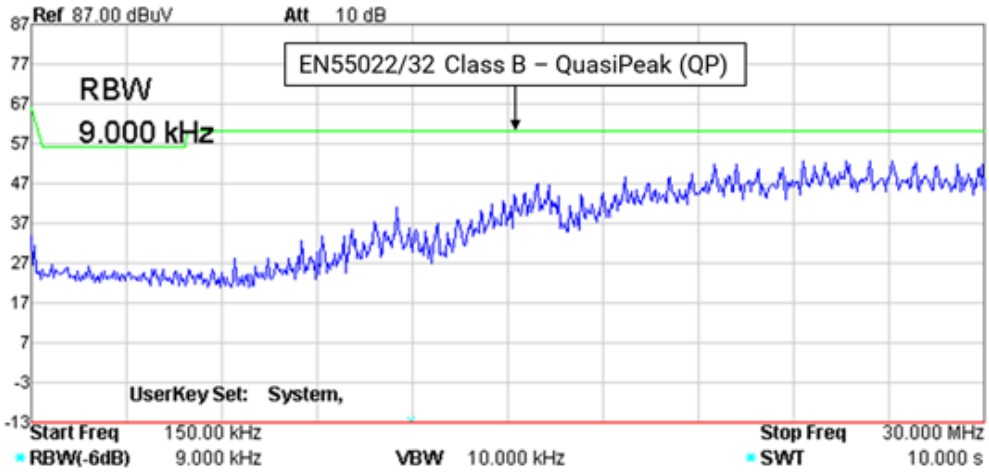

Figure 5 – Conducted EMI noise of the 3-level totem-pole PFC with two-stages EMI filters

These advantages have been realised in a range of designs, with “nameplate” ratings between 300W and 3kW. Typically, in a multilevel approach the costs of silicon will be comparable – but the key challenge is associated with effecting low-cost and precise gate drives, with “normally off” operation and zero quiescent current. These have been implemented effectively as cells with complementary magnetic drive usage for high performance in a repeatable component at low cost.

The practicality of implementation is also reliant on effective digital controllers, with the ability to provide pulse drives as needed by these cells.

It is important to “compare and contrast” these approaches with interleaved power conversion stages, which usually use two of the “classic” boost stages of Figure 1 operating in parallel but with 180° drive phase shift. Such stages can cancel ripple at the input to the converter, but require dual inductors with high volt-seconds applied, as well as having high-voltage switching. This compares with the small inductor and lower-voltage switching that is feasible with a stacked-multi-phase approach.

5. Current and Voltage Sensing

Usage of all-isolated gate drives allows resistive current sensing without “contamination” from drive signals. Central current sampling – i.e. at the midpoint of the conduction phase of the lowest device – can allow the average current value to be determined readily.

Availability of low-current operational amplifiers allows differential sensing of input voltage, differential sensing of flying capacitor voltage, and conventional resistive approaches used for output voltage. Dual sensing of output voltage can be used for protection. Comparator approaches also allow rapid identification of input voltage polarities, giving the ability to independently control line synchronous rectification (SR) MOSFETs and consequently prevent reverse power flow under fault conditions.

6. Summary

ICERGi is introducing a new paradigm for power factor correction circuitry in high-volume ACDC deployments. Alignment of topology, component engineering and control enhancements gives power system designers and architects the opportunity to implement physically small, high efficiency circuitry for this key PFC function.

Revision History

Date	Version	Changes
05-12-2015	1.0	First release
05-08-2019	1.1	Updated and corrected Figures 1, 2, 3, and 4 Added Figure 5 – Conducted EMI noise data Updated power ratings in Section 3 and 4 Update voltage and current sense approaches in Section 5