Stack Multiphase Asymmetrical Half-Bridge Topology Offering Advance Performance and Efficiency

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Abstract— **In quest of higher efficiency and power density, various studies have been carried out to boost the performance of conventional asymmetrical half bridge (AHB) topologies through either magnetics optimization or deployments of fully soft switching schemes. Although the reporting results from existing works are quite promising, none of them show significant breakthrough in power conversion density which is currently limited by existing technologies for high-voltage (above 500V) MOSFETs. This paper proposes a novel stacked multiphase asymmetrical half bridge (SMAHB) topology operating in a similar manner as conventional AHB converters, but enabling deployment of 250V MOSFETs for faster switching and material reduction in magnetics and EMI filters, which allows high efficient and compact implementation. The operation and performance of the proposed converter is confirmed via both simulated and experimental data.**

Keywords— AHB; multi-cell conversion; high power density; Isolated DC-DC conversion

I. INTRODUCTION

AHB converters belong to a class of soft-switching converters, but operate with a fixed switching frequency [1], [2]. The resonant tank is fundamentally formed by parasitic components of main switching devices and transformer; hence, implementation is generally simple with minimum requirement on magnetics and EMI filter design. AHB converters are mainly used after PFC rectifiers with an output voltage of around 400V for nominal operation and up to 450V for transient responses; so the main MOSFETs used for implementation must have voltage ratings above 500V if a tolerance of 20% is taken into account. Switching characteristics of high voltage MOSFETs are far from ideal and in consequence imposes a bottleneck on converter performance and power density even with optimized magnetics [3] - [5] or fully soft switching [6]. Therefore, it is desirable to develop a new AHB topology that can eliminate such constraints while retaining all desired properties of conventional ones.

Generally, boosting switching frequencies is an effective way to shrink the size of passive components, such as transformer and filters; however; switching losses are too great to be handled by existing silicon switching devices. Using GaN FETs for implementation could be a worthy solution here [7]; however it is costly and likely less reliable as compared to silicon-based ones. One possible solution is to rely on multi-cell topologies [8], [9], allowing not only magnetic volume reduction through current ripple cancelation but also the deployment of low-voltage MOSFETs for faster switching and lower losses.

Multilevel conversion techniques have been widely adopted in high voltage and high power DC-to-AC inverters and DC-to-DC choppers, where a single switching device either is unable to handle a significant voltage swing, for example over 5kV, or cannot provide adequate performance in terms of speed, efficiency and electro-magnetic interference (EMI). The key purposes of multilevel approaches are to use multiple switches for evenly sharing the voltage stress, which allows the deployment of lower voltage rating but faster switching devices.

Although many studies have been conducted to develop multi-level topologies for isolated DC-DC applications from various basic topologies including both soft-switching hard-switching converters [10] - [13], there is no research concerning multi-cell deployment for AHB topologies and making use of 250V MOSFETs as main switches for implementation of mid-power isolated DC-DC converters. Therefore, the man objective of this paper is to address all mentioned challenges.

II. PROPOSED STACKED MULTIPHASE-ASYMMETRICAL HALF-BRIDGE CONVERTER

Multilevel conversion techniques have been successfully adopted in various DC/AC and AC/DC topologies to reduce the voltage stresses on switching devices, so it is logical to borrow the same principle and apply it to conventional AHB converters. Figure 1 illustrates a result obtained by replacing a conventional voltage chopper with a three-level switching stage [9] while keeping the remaining structure of the converter unchanged. The two input capacitors C_{in1} and C_{in2} generate a bypass mid-point voltage of $V_{in}/2$ which defines the voltage stresses on the main switching devices when going through their cycle of operation. The capacitor C_b acts as an energy storage and DC blocking device while the center-tapped transformer provides galvanic isolation and voltage transformation.

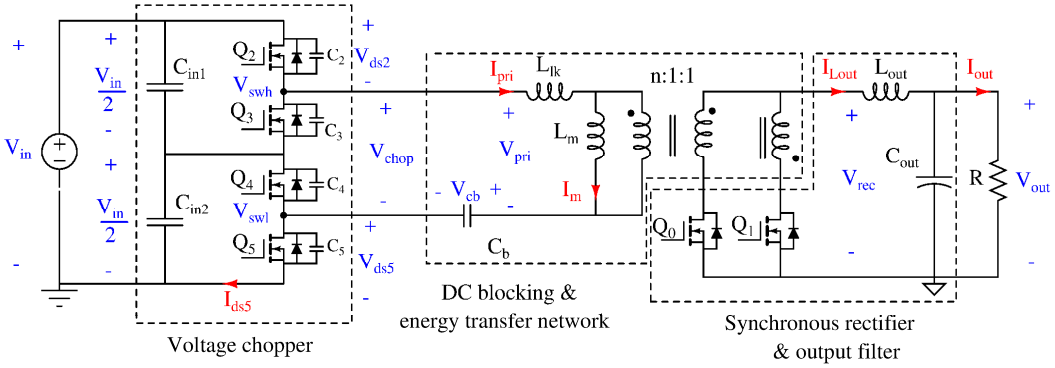

Fig. 1: Circuit diagram of the proposed stacked multiphase AHB converter

The leakage inductance L_{lk} of the transformer and internal capacitance C_2, C_3, C_4 and C_5 of the primary switching devices form a resonant tank whereby the energy stored in L_{lk} can be recycled to bring the drain-source voltages of MOSFETs to zero before they are turned on, i.e. ZVS. Two active switches at the secondary play the role of a synchronous rectifier (SR) feeding the output filter formed by an inductor and an electrolytic capacitor.

The proposed circuit as shown in Fig. 1 inherit the operating principle of the original AHB converter. Particularly, the input voltage is first processed by the voltage chopper which outputs a square wave signal having an amplitude of $V_{in}/2$ and a frequency of twice the switching frequency of the main MOSFETs. The square wave voltage then has its DC component removed when travelling further downstream and is amplified by the transformer. The pulse signals appearing at the transformer secondary terminals are then rectified by the SR, and subsequently filtered out by the output inductor L_{out} and output capacitor C_{out}.

Although the proposed converter looks very similar to that of the work presented in [11], one can easily confirm in Section III that a different modulation scheme is deployed in this paper, and, as a consequence, operating principle is not quite the same.

III. OPERATIONAL PRINCIPLES

Keeping the mid-point voltage balanced is the key point in sustaining voltage stresses evenly between primary switches; therefore, the modulation pattern should facilitate such a target. In particular, the top MOSFET Q_2 is paired with Q_3 while Q_4 is paired with the bottom MOSFET Q_5. Each of paired switches is driven in a complementary manner, i.e. when one switch of the pair is on, the other must be off and vice versa. The PWM control signals for Q_2 and Q_5 share the same duty ratio (1-D) and switching frequency f_{pwm}, but are different in phase by an angle of 180 degrees. In order to facilitate ZVS, a small dead-time is introduced between on-off transitions of each complementary pair of switches. For SR, Q_0 is set on when either Q_2 or Q_5 is on while negating the driving pulse for Q_0 gives that of Q_1. Figure 2 illustrates the driving sequence for all switches in the proposed AHB converter, and resulting voltages and currents along the power transfer path. Thanks to the switching pattern, the output-to-input voltage ratio is simply controlled by the variable D which is defined as the duty ratio of the middle MOSFET Q_4.

The proposed converter has four main operating phases interleaved with four switch-transition phases during each switching cycle, which is highlighted by the timeline from t_0 to t_8 as highlighted in Fig. 2. Since the switching pattern is repeated within a cycle, only the first four sequential states are described in details.

- **Main phase 1 ($t_0 \sim t_1$)**: power transfers from the capacitor C_{in2} to the output through Q_3, Q_5 and Q_0, and charge C_b. Voltage across the primary side of the transformer is $V_{in}/2 - V_{cb}$.
- **Transition phase 2 ($t_1 \sim t_2$)**: since Q_5 is turned off at t_1, the primary current I_{pri} will start charging C_5 and discharging C_4 until $V_{C4} = V_{Cb}$. After this time instant, the secondary side of the transformer is decoupled from the primary side. The output inductor current freewheels through both SR Q_0 and Q_1 while the capacitor C_4 continues to be discharged by the energy stored in L_{lk}. only The body diode of Q_4 starts conducting when C_4 approaches zero, which allows ZVS if turning Q_4 on is triggered when such a condition is still maintained. Although both Q_4 and Q_3 now are on, there is still no energy transferring to the secondary side until $I_{pri} - I_m = -I_{out}/n$ which happens at $t = t_2$.
- **Main phase 3 ($t_2 \sim t_3$)**: the blocking capacitor now connects to the primary side of the transformer in a reverse polarity fashion, which allows power stored in C_b transferring to the output. Voltage across the primary side of the transformer is $-V_{cb}$ which appears at secondary side as V_{cb}/n.
- **Transition phase 4 ($t_3 \sim t_4$)**: Q_3 is switched off at $t = t_3$, which forces the primary current to go through the internal capacitor of Q_3. This action will ramp up the voltage across C_3 and simultaneously ramps down V_{C2}. When $V_{C3} > V_{Cb}$, the secondary side of the transformer is again

decoupled from the primary side until $t = t_4$. As mentioned in Transition phase 2, ZVS for Q_2 is also achieved if its gate drive signal is kicked in after the primary current change its polarity.

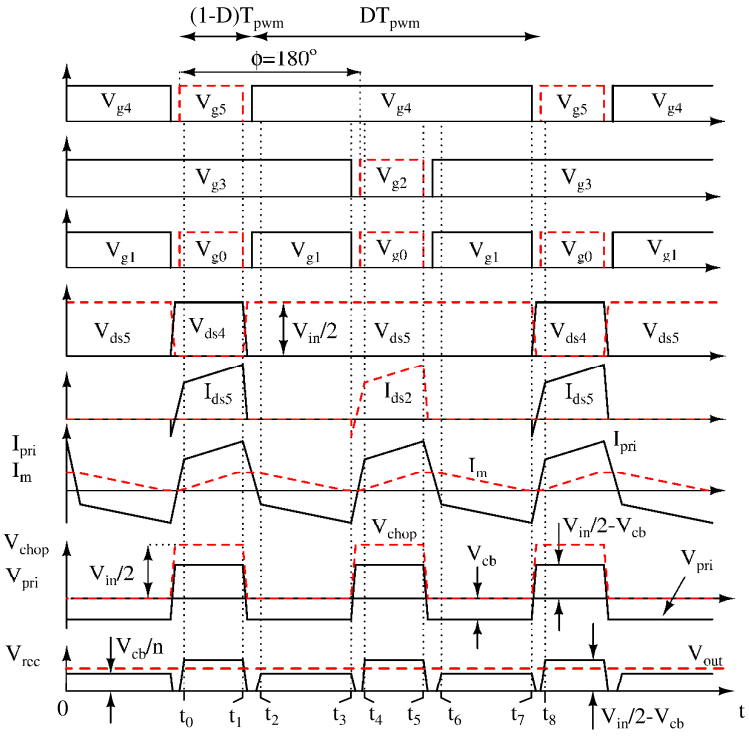

Fig. 2: Key operating waveforms of the proposed stacked multiphase AHB converters

Fig. 2 shows that the SMAHB converter has the same operational voltage and current waveforms as a conventional AHB converter with a switching frequency of $2*f_{pwm}$. and an input voltage of $V_{in}/2$ This implies that the use of a multi-level voltage chopper here does not alter the way that the converter operates, it simply doubles the operating frequency of magnetic components and reduce the converter gain by half. The effect on the conversion gain is actually trivial as one can easily compensate for such reduction by doubling the transformer ratio.

IV. CONVERTER CHARACTERISATION

Like any conventional AHB converter, the following assumptions are made to simplify the DC analysis of the proposed converter [2]:

- All components are ideal and do not incur any loss
- The leakage inductance L_{lk} is much smaller than the magnetizing inductance L_m
- The blocking capacitor voltage V_{Cb} has negligible ripples and can be considered as constant during each switching cycle.

A. *Input-to-output-voltage gain*

If the duty cycle loss due to transformer decoupling during transition phases is negligible, the output voltage can be calculated by averaging the rectifier voltage over time as given by

$$V_{\text{out}} = \frac{2(1-D)}{n}\left(\frac{V_{in}}{2} - V_{cb}\right) + \frac{2(D-0.5)}{n}V_{cb}. \quad (1)$$

where D denotes the duty ratio of Q_4, and is assumed to be limited to [0.5 1] while n is the turn ratio of the center-tapped transformer. V_{in}, V_{out} and V_{cb} denotes the input voltage, output voltage and blocking capacitor voltage, respectively. Applying the volt-second balance to the primary transformer winding gives

$$2(1-D)\left(\frac{V_{in}}{2} - V_{cb}\right) - 2(D-0.5)V_{cb} = 0. \quad (2)$$

Solving (2) for the blocking capacitor voltage yields

$$V_{cb} = (1-D)V_{in}. \quad (3)$$

Substituting (3) into (1) and solving for the input-to-output gain gives

$$G_{io} = \frac{V_{out}}{V_{in}} = \frac{2(1-D)(2D-1)}{n} \quad (4)$$

Figure 3 plots the voltage gain of the proposed converter as a function of the duty ratio D and the transformer turn ratio. For any value of n, the gain curve is symmetrical around 75%, which suggests that controller design should limit the dynamic range of D to either [0.5 0.75] or [0.75 1]. Technically, operation range above 75% is preferable as this allows lower operating voltage for the blocking capacitor.

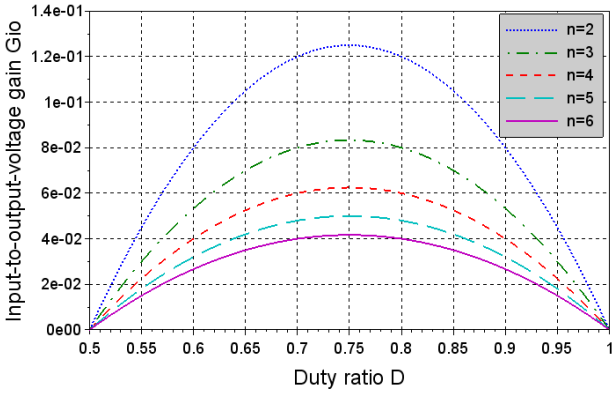

Fig. 3: DC voltage gain of the SMAHB converter

Although (4)seems to be fine for ballpark calculations, a more accurate design should include the amount of duty cycle stolen by the resonant tank for ZVS as described by (5)

$$V_{out} = \frac{2(1-D)(2D-1)}{n} V_{in} - \frac{8 I_{out} L_{lk}}{n^2 T_{pwm}}, \quad (5)$$

B. DC current and ripples

Since the sum of charge of C_b over one switching cycle equals zero at steady state, the magnetizing current is required to balance out the current withdrawn by the load, which implies

$$2(1-D)\left(I_m + \frac{I_{out}}{n}\right) + 2(D-0.5)\left(I_m - \frac{I_{out}}{n}\right) = 0. \quad (6)$$

Solving (6) for I_m gives

$$I_m = (4D-3)\frac{I_{out}}{n}. \quad (7)$$

Given the voltage across L_m and L_{out} as V_{pri} and $V_{rec} - V_{out}$, respectively, the magnetizing current and output current ripple can be calculated via

$$\Delta I_{m\_pp} = \frac{V_{bulk}(D-0.5)(1-D)T_{pwm}}{L_m} \quad (8)$$

$$\Delta I_{Lout\_pp} = \frac{(1-D)T_{pwm}}{L_{out}}\left(\frac{(D-0.5)V_{in}}{n} - V_{out}\right) \quad (9)$$

C. ZVS conditions

After Q_2 is turned off, C_3 is discharged from V_{cb} to 0V by the energy storage in L_{lk}. Therefore, the ZVS condition for Q_3 is equivalent to

$$\frac{1}{2} L_{lk} I_{pri\_peak}^2 > \frac{1}{2}(C_2 + C_3) V_{Cb}^2, \quad (10)$$

where I_{pri_peak} denotes the peak of the primary current which can be approximated by

$$I_{pri\_peak} \approx \frac{I_{out}}{n} + I_m + \frac{\Delta I_{mpp}}{2}. \quad (11)$$

Similarly, the ZVS condition for Q2 requires that C2 is fully discharged from $V_{in}/2 - V_{cb}$ by the energy stored in the leakage inductance only Such a condition can be mathematically expressed by

$$\frac{1}{2} L_{lk} I_{pri\_valley}^2 > \frac{1}{2}(C_2 + C_3)\left(\frac{V_{in}}{2} - V_{cb}\right)^2, \quad (12)$$

where I_{pri_valley} indicates the valley of the primary current which can be approximated by

$$I_{pri\_peak} \approx -\frac{I_{out}}{n} + I_m - \frac{\Delta I_{mpp}}{2} \quad (13)$$

V. DESIGN AND IMPLEMENTATION

The design specifications for a SMAHB converter prototype are listed in TABLE I.

TABLE I: CONVERTER DESIGN SPECIFICATIONS

Input voltage, V_{in}	$360V_{DC}$-$400V_{DC}$
Nominal output voltage, V_{out}	$12V_{DC}$
Switching frequency, f_{pwm}	200kHz
Maximum output power, P_{out_max}	200W
Maximal inductor current ripples ΔI_{Lout_max}	2.1A
Hold-up time, t_{holdup}	20ms

A. Power stage design

1) Center-tapped Transformer desgin:

As observed in (5), the presence of the duty cycle loss complicates the selection of the transformer ratio n as the leakage inductance is an also unknown variable here. Therefore, it makes sense to use (4) for initial design calculations and (5) for validation purposes.

Given the minimal input voltage of 360V and the output voltage of 12V, the transformer turn ratio should be chosen to

provide a maximal voltage gain of at least 0.033. According to the set of gain curves as shown in Fig. 3, an optimal value for n should be 6.

The leakage inductance is chosen to ensure that (5) is satisfied at minimal input voltage and maximal load, i.e.

$$L_{lk} \le \frac{n^2 T_{pwm}}{8 I_{out\_\max}} \left[\frac{2(1-D_{\min})(2D_{\min}-1)}{n} V_{in\_\min} - V_{out} \right] \le 3.8uH$$

Considering a margin of 20% gives L_{lk} = 3uH. The magnetizing inductance value influences the peak and valley current levels which indirectly affect the ZVS condition. Therefore, L_m can be designed to ensure ZVS from full load to 20% max load. Firstly, the duty ratio for 20% load can be approximated by

$$D_{20\%} = 1 - \frac{1 - \sqrt{1 - \frac{4nV_{out}}{V_{bulk}}}}{4} = 0.88 \quad (14)$$

The maximum magnetizing inductance value ensuring ZVS is given by

$$L_{m\max} = \frac{V_{in}(D_{20\%} - 0.5)(1 - D_{20\%})T_{pwm}}{\sqrt{\frac{C_2 + C_3}{L_{lk}} \frac{V_{in}^2}{4}} - \frac{I_{out}}{n} + \frac{(4D_{20\%} - 3)I_{out}}{n}} = 93\mu H \quad (15)$$

For implementation, L_m is chosen to be 65uH.

2) Output inductor design

Given the maximal ripple requirement, the output inductor can be calculated via

$$L_{out} = \frac{(1-D)T_{pwm}}{\Delta I_{Lout\_pp}} \left(\frac{(D-0.5)V_{in}}{n} - V_{out} \right) = \frac{(1-0.88)5e-6}{2.1} \left(\frac{(0.88-0.5)400}{6} - 12 \right) = 3.8uH \quad (16)$$

3) Switching device selection

The switching waveforms as shown in Fig. 1Fig. 2 confirms that the operating voltage of the primary FETs is only half of the input voltage, suggesting that it is possible to employ 250V MOSFETs for implementation because the nominal output voltage of an PFC stage is typically set around 400V.

B. Implementation

The design procedure as discussed in Section V.A suggests the following components: L_{out}=3.8uH, C_{out} = 1500uF – 16V rating- electrolytic, C_{in1} = C_{in2} = 220nF - 250V rating - ceramic. The center-tapped transformer has a turn ratio of 12:2:2 with the magnetizing inductance of 65uH and the leakage inductance of 3uH. The main switches are BSC16DN25 with 250V rating and on resistance of 165mΩ, and controlled by ARM Cortex M0 (STM32F051) through proprietary isolated gate-drive circuitry

VI. EXPERIMENTAL RESULTS

Operational waveforms at 400V input voltage and load powers of 100W are illustrated in Figures 3 and 4. The experimental results show that the converter allows ZVS similar to AHB converters but has only a half of voltage stress on the main switching devices, which confirms the feasibility of the deployment of 250V MOSFETs. Although the efficiency data is not available at the time of writing this paper, it is expected to achieve a figure as high as 97%.

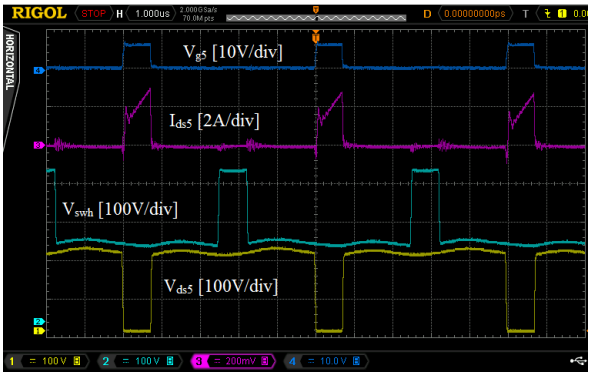

Fig. 4: Operational waveforms of the proposed SMAHB converter at V_{in} = 400V and P_{out} = 100W: (CH1) V_{ds5} – Drain source voltage Q5, (CH2) V_{swh} – High side switched node, (CH3) I_{ds5} – Q5 current, (CH4) V_{gs5} – Gate drive of Q5

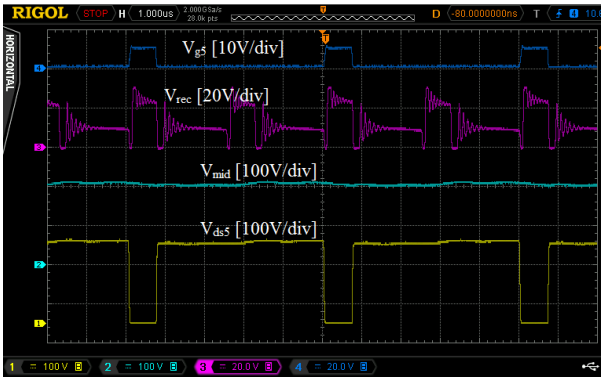

Fig. 5: Operational waveforms of the proposed SMAHB converter at V_{in} = 400V and P_{out} = 100W: (CH1) Drain source voltage Q5, (CH2) V_{mid} – Midpoint capacitor voltage, (CH3) V_{rec} – Rectified secondary voltage, (CH4) V_{gs5} – Gate drive of Q5

VII. CONCLUSIONS

This paper developed a new stacked multiphase AHB topology inheriting not only zero voltage switching from traditional AHB converters but also low voltage stresses and ripples cancelation from multilevel power conversion, allowing material reduction in magnetic sizes, EMI filters, and product volumes, and especially facilitating deployment of 250V-type MOSFETs as main switches. Although implementing the proposed converter requires more switching devices as compared with traditional solutions, the efficiency and final costs of the design are not compromised. Therefore, the new topology is well suited to economical and compact realization of isolated DC-DC converters to be operated with a maximum input voltage of 450V and output power ranging from 70W to 2kW. The common application is after the PFC stage in two-stage power supplies.

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