Practical Switching Frequency Control for Improved Efficiency in CCM Boost PFC Converters at Light Load

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***Abstract* — Existing control methods in continuous conduction mode (CCM) boost PFC topologies employ a fixed switching frequency over the whole range of operation. Besides a simple implementation, retaining the switching frequency unchanged, places front stage converters at a suboptimal level during light load operating conditions. In particular, the dominant switching loss can often lead to an adverse impact on the systems efficiency. This paper proposes a novel control approach to both optimize the light load efficiency and improve input current regulation issues associated with a switching frequency adjustment. The control method is verified using a 3kW bridgeless totem-pole PFC prototype delivering a substantial switching loss reduction enabling 99% power conversion efficiency even with diode rectification.**

Keywords — switched gain current sense amplifier, digital switching frequency control, hard switching, bridgeless totem-pole, multi-level, power factor correction (PFC).

I. Introduction

Switching losses are the dominant loss mechanism in hard switching PFC converters during light load operation. This observation also holds true for bridgeless totem-pole PFC topologies using either wide band gap (WBG) devices [1], [2] or low voltage power MOSFETs even though the later implementation offer 4x reduction in magnetic size and lower losses [3]. Due to the inherent hard switching behavior using CCM and a fixed switching frequency, the efficiency of the converter is compromised at lower power levels. In general, semiconductor (Si, SiC or GaN) power loss consists of three major components: conduction loss, switching loss and driving loss. Conduction loss is always present, however, does not have a significant impact at lower power. In contrast, both frequency dependent switching and drive power dominate the loss budget. The power expenditure is increased even further in a case of hard switching and (of course) higher switching frequency. This poses a serious challenge in order to meet the most stringent efficiency requirements for a front-end converter. For instance, the efficient energy use standards required for PSUs to meet the titanium or diamond level certifications imposed by programs such as 80 PLUS [4] or ETA [5].

Moreover, to achieve the cost-parity between the conventional boost PFC and the 3-level BTP platforms, the design must employ a diode bridge in rectification stage. This constitutes a greater design challenge to achieve very high efficiency due to a fixed diode forward voltage drop as opposed to the more costly actively controlled switches. The primary objective of this paper is to demonstrate a method to improve a front-end converter stage that can offer both the highest efficiency (η_{peak} > 99%) and the cost-parity with the conventional design while maintaining high PF and low ATHD at low to medium power levels.

Several efficiency saving techniques at low power have been proposed to solve a similar issue [6], [7] however, at the cost of higher complexity or additional tradeoffs. Lowering the switching frequency at low power to boost the efficiency is a potential solution. Despite that, it poses several design and frequency control challenges that must be considered for effective and reliable implementation. Some of the major hurdles to overcome are as follows: timing in a switching frequency transition, adaptive controller for different system dynamics, good inductor current shaping, switched current sense gain for higher program current resolution, etc. Thus, there is an urge to develop a practical and versatile frequency controller that can improve the converting efficiency for a front-end stage at low power. The control method should be scalable and not limited to a fixed set of switching frequencies that can be exploited in a variety of different hard-switched applications such as the conventional boost, bridgeless totem-pole, etc.

II. Overview of the 3-Level Bridgeless Totem-Pole PFC Topology

Fig. 1 below illustrates the high-level circuit diagram of the 3-level bridgeless totem-pole PFC [8]. The multilevel converter consists of a line frequency diode bridge rectifier D_{1-2}, main PFC inductor L, high-frequency switching leg Q_{1-8} with an additional flying capacitor C_{Fly} for voltage division and output capacitor C_{Bulk}.

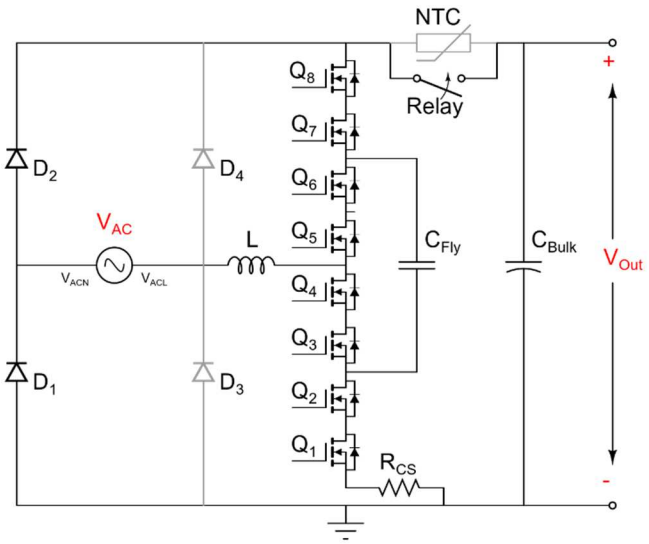

Fig. 1: High level circuit diagram of a 3-level bridgeless totem-pole PFC

The flying capacitor voltage initialization and balancing is achieved by a hybrid balancing method proposed in [9]. The inrush current during the startup is handled by an NTC thermistor which is subsequently bypassed with a relay during a steady state operation. A set of bypass diodes D_3 and D_4 allow for an alternative low impedance path to charge the output capacitors during startup. In this manner, high magnitude current is diverted away from both the PFC inductor and the high-frequency switching leg devices during the start up or input surge events.

A. Principle of Operation

Bridgeless totem-pole PFC operates in positive (D_1 forward biased) and negative (D_2 forward biased) half line cycles of the AC mains input. The 3-level high-frequency MOSFET string is controlled using a phase-shift modulation (PSM) with a nominal switching frequency of 66 kHz. Each pair of devices (i.e., Q_1 and Q_2) share the same drive signal. In addition, $Q_{1\text{-}2}$ together with $Q_{7\text{-}8}$ as well as $Q_{3\text{-}4}$ together with $Q_{5\text{-}6}$ pairs are complementarily driven. The control signals of $Q_{1\text{-}2}$ and $Q_{3\text{-}4}$ share the same duty ratio D and switching period T_{PWM}, but with the offset in phase angle of 180°. Fundamentally, the converter regulation consists of two feedback loops. The average output DC voltage is regulated by a slow response outer loop, whereas the inner loop responsible for shaping the input current is a much faster loop. The instantaneous output voltage (V_{Bulk}), flying capacitor voltage (V_{Fly}) and input voltage (V_{AC}) signals are sensed and conditioned by external voltage amplifier circuits which are then fed back to the microcontroller. The average inductor current is programmed using a low side current sense amplifier that measures the voltage across a resistor R_{CS} connected between Q_1 and ground.

B. Power MOSFET Loss Analysis

Given the application with hard switching, power MOSFET devices are carefully selected based on several parameters such as drain-to-source resistance $R_{DS(ON)}$, gate charge Q_g, reverse recovery charge Q_{rr}, output charge Q_{oss}, etc. Reverse recovery characteristics are particularly important in a hard switched converter design and its efficiency. Therefore, to minimize the effect of an intrinsic body diode and to improve the overall efficiency of the system, power MOSFETs with lower reverse recovery time t_{rr} as well as Q_{rr} are a preferred option. Among the commercially available 150V-rated MOSFET products, using Infineon's BSC093N15NS5 devices with on-resistance of 9.3 mΩ allows for the optimal price to performance ratio of the boost stage with the output load up to 3000W.

1) Conduction Loss

The conduction loss is mainly a function of the combined on-resistances of all conducting devices. It is worth mentioning that there are 4 MOSFET devices turned on at any given instant during a steady state operation. Thus, the conduction loss (CCM) over a one switching period can be calculated as follows:

$$P_{cond} = 4 \cdot \left(I_{L_{RMS}}^2 \cdot R_{DS(ON)\ @\ 80°C}\right) \tag{1}$$

C. Switching Loss

The active HF switching leg consists of two phases 180° apart from each other. Switching loss for each device occurs in both transitions (Fig. 2).

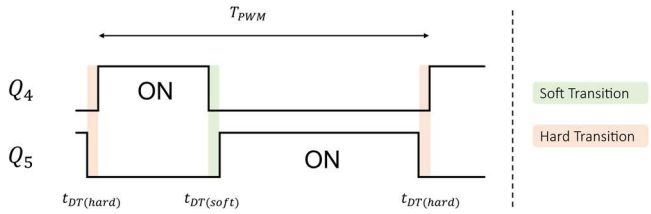

Fig. 2: Switching waveforms

The time when Q_4 is switching off and Q_5 is switching on results in a soft transition accompanied with an adequate dead time and thus can be ignored for the sake of the loss analysis. On the contrary, the opposite instant leads to a hard switched transition. As soon as Q_5 is switched off, its intrinsic body diode gets forward biased to allow for continuous inductor current flow until Q_4 is fully enhanced. During this instant the inductor current must change its direction immediately, however, inability to prevent the reverse current for a certain amount of time leads to abruptions and the associated power losses in the device. Given the fact that the same switching frequency, duty ratio and a perfect voltage sharing between all devices are satisfied, the total switching loss can be estimated as follows:

$$P_{switch} = 4 \cdot \left(P_{VI(Overlap)} + P_{C_{oss}} + P_{chargeC}\right) \tag{2}$$

$$P_{VI(Overlap)} = V_{bulk} I_L (t_1 + t_2) \,/\, 8T_{pwm} \tag{3}$$

$$P_{C_{oss}} \approx P_{chargeC} = V_{bulk} Q_{oss} \,/ 4T_{pwm} \tag{4}$$

1) Drive Loss

The PWM signal is delivered to each of the MOSFET devices in a string using an isolated gate driver. The energy required to drive each device in a string depends on its input capacitance. Thus, for a single phase the total gate drive loss for all 8 devices can be calculated as follows:

$$P_{drive} = 8 V_G Q_G \,/\, T_{PWM} \tag{5}$$

Based on the list of formulas provided above, lowering the switching frequency can help to reduce losses in the PFC boost stage at light to medium load. In particular, halving the fundamental switching frequency from 66 kHz down to 33 kHz can half both the switching loss and drive loss of the HF switching leg. This is a particularly appealing feature that the multilevel converter can benefit from thanks to the inherent frequency multiplication of the effective inductor current ripple with respect to the switching frequency. Combining the computed switching and drive loss yields the estimated loss reduction of around 2.2W (average) up to 1 kW output load. However, while extremely efficient at low power, the solution must be carefully implemented at intermediate power levels without compromising EMI requirements.

III. Frequency Control in Bridgeless Totem-pole PFC

The proposed switching frequency control block diagram is depicted in Fig. 3. It consists of three major elements such as isolated gate drivers (green), external current and voltage sensing amplifiers (orange), and the embedded microcontroller environment (blue).

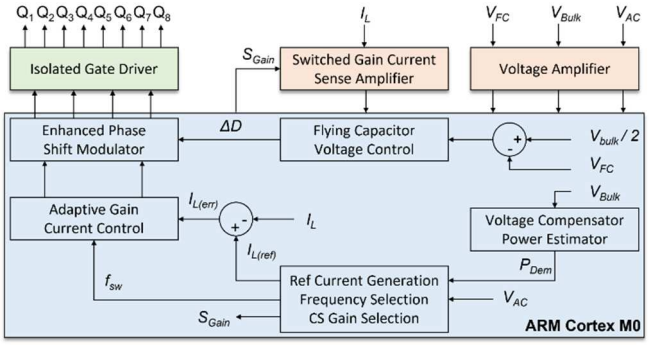

Fig. 3: Proposed digital frequency control block diagram for 3-level bridgeless totem-pole PFC converter

A. Frequency Selectoion

Switching frequency selection is governed by demand power parameter P_{dem}. It is computed and updated between each half line cycle. During the steady state operation, it is estimated based on the output voltage V_{Bulk} and subsequently averaged to achieve a slower response between the intermediate power levels. In addition, frequency adjustment is a function of input voltage V_{AC} which helps to differentiate and manage power levels according to various user defined input voltage levels. In other words, the frequency control action can be implemented for both low-line and high-line input voltages independently. Halving the switching frequency to 33 kHz reduces both the switching loss and the drive power, however, it gives rise to slower current loop control dynamics.

B. Adaptive Gain Current Control

To overcome this challenge, the adaptive gain current control is implemented to adjust the PI gain parameters. It acts on both the input current error $I_{L(err)}$ and the switching frequency f_{sw}. In this manner, the PI compensator can be configured with larger proportional and integral gains to account for slower current loop dynamics. It is important to emphasize that while the current control action is taken on a switching cycle basis, the frequency parameter f_{sw} is only updated at input voltage zero crossing. However, lowering the switching frequency can potentially lead to poor input current THD and power factor of the system. This is more evident at low power during which the current amplitude is relatively low impacting the inductor current regulation.

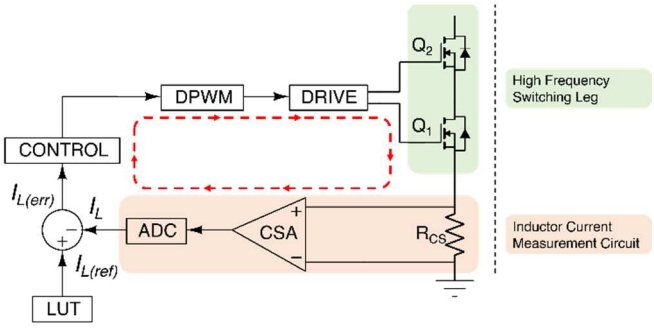

Fig. 4: Inductor current measurement with low-side current sense resistor R_{CS}

The inductor current is measured with a low-side current sense resistor connected between ground and Q_1 (Fig. 4). The signal from a single-supply current sense amplifier across R_{CS} is sampled and processed by a microcontroller during the time both Q_1 and Q_2 are ON. However, small voltages developed across the shunt resistor during a light load operation can be misinterpreted due to a poor signal to noise ratio (SNR). The unwanted noise does not have a single well-defined source, instead it can be realized as a combination of switching transitions, inductor current measurement loop, ADC resolution and quantization error. Even though the inductor current is sampled at the midpoint when both Q_1 and Q_2 are on for any given duty ratio, the switching action is still present in the system due to hard switching in a totem-pole arrangement. Moreover, due to limitations in ADC resolution, low input current can result in measurement inaccuracy considering the appropriate scaling to account for a full range of inductor current. In the case of 10mΩ shunt resistor R_{CS} and a 12-bit ADC with an offset of 2048 counts for positive and negative inductor current measurement, 1A of instantaneous current corresponds to 62 ADC counts. The converter operated with the input voltage $V_{IN} = 230V_{AC}$ and the output power $P_{OUT} = 100W$ equates to inductor RMS current $I_{L(RMS)}$ of 0.45A ($I_{L(Peak)} = 0.65A$). Assuming a measurement noise in the order of several ADC counts, it could potentially distort the inductor current measurement up to 15% of the real value. The controller can be updated with an increased gain, however, as the control gain becomes larger, issues arise with the amplified unwanted noise entering the system potentially causing the instability of a feedback loop.

C. Switched Gain Current Sense Amplifier

To mitigate these concerns, a switched gain current sense amplifier is implemented as a part of a switching frequency control architecture. Fig. 5 demonstrates the circuit diagram of such implementation.

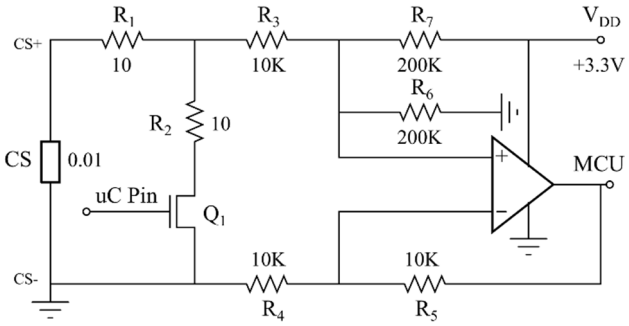

Fig. 5: Circuit diagram of switched gain current sense amplifier arrangement

The signal across the current sense resistor to the amplifier circuit is controlled with a single low-side NMOS device Q_1 which is directly driven from a microcontroller. At its most basic form, the voltage divider consisting of resistors R_1 and R_2 is toggled to provide two discrete gain settings. During the time Q_1 is on, the current sense voltage is divided by a half. On the contrary, when Q_1 is off, the signal is directly fed to the differential amplifier. Note that resistors R_6 and R_7 provide a voltage offset of 1.65V to the non-inverting input of the differential amplifier so that both positive and negative current sense voltages can be measured. Given this arrangement, the relationship between input and output of the current sense amplifier circuit during the time Q_1 is off (1) and on (2) can be calculated as follows:

$$V_{Out} = 1.65V + \frac{100k\Omega}{10k\Omega} * (V_{CS+} - V_{CS-}) = 1.65V + \mathbf{10} * V_{CS} \quad (6)$$

$$V_{Out} = 1.65V + \frac{100k\Omega}{10k\Omega} * \frac{(V_{CS+} - V_{CS-})}{2} = 1.65V + \mathbf{5} * V_{CS} \quad (7)$$

Using a larger current sense resistor in conjunction with higher gain, (6) of the amplifier improves the signal resolution due to an increased voltage developed across R_{CS} for the same amount of current flowing through it. Since the amplification of the signal is achieved on the input side of the operational amplifier, noise has minimum to no scaling applied to it. This allows for a greater SNR substantially improving power factor correction due to a minimized input current THD and overall improvement in front-stage system stability. The equations above apply to different load conditions. The adequate ADC margin must be considered to take power loss as well as input current protection level into consideration when deciding on the operating range of the proposed control arrangement. In 3kW PFC application, the proposed switching frequency control method can be extended up to half of the rated maximum load, namely, 1500W at $230V_{AC}$ and 750W at $115V_{AC}$. Once the output power is above the predefined threshold, the current sense amplifier gain can be reduced (7), thereby allowing for a sufficient dynamic range during high input current operation.

IV. Simulation

The proposed switched gain current sense amplifier circuit is simulated and verified using the LTSpice simulation software (Fig. 6). The selected simulation components agree with those of real word implementation. The attenuation of the current sense voltage is controlled with a 20V NMOS device (DMN2400UFD). Subsequently, the signal is fed to a 3V single rail 80MHz operational amplifier (OPA358).

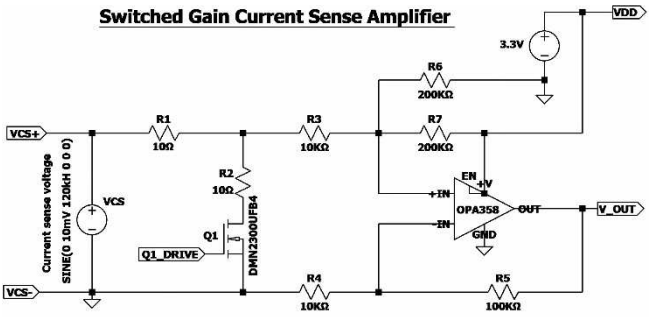

Fig. 6: Switched gain current sense amplifier circuit simulation (LTSpice).

For this simulation, an emulated current sense resistor AC voltage $V_{CS} = 10mV_{(Pk\text{-}Pk)}$ with double of the effective inductor switching frequency of 120kHz is subjected to the system. Once Q_1 is switched off, the gain is increased resulting in the output signal of the differential amplifier to double from $50mV_{(Pk\text{-}Pk)}$ to $100mV_{(Pk\text{-}Pk)}$ (Fig. 7). Any potential noise present between the voltage divider network R_1, R_2 and the input to a microcontroller does not undergo additional amplification which combined with a greater resolution can substantially improve the inductor current shaping during light to medium load operation.

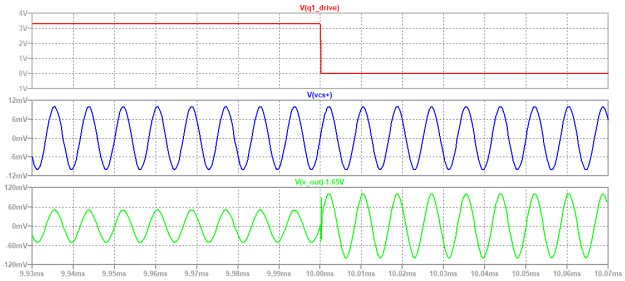

Fig. 7: Simulation results of switched gain current sense amplifier arrangement. Q_1 control signal (RED), voltage across R_{CS} (BLUE), current sense amplifier output without an offset of $V_{DD}/2 = 1.65V$ (GREEN)

V. Experimental Results

The proposed digital frequency control architecture is implemented using a low-cost ARM Cortex M0 microcontroller and a set of additional operational amplifier circuits. It is verified using a diode-based 3kW bridgeless totem-pole PFC prototype (Fig. 8) with a corresponding BOM depicted in Table I. The benchmark data with a peak high-line efficiency η_{peak} above 99% and η_{peak} = 98% at low-line are captured in Fig. 9 below.

Fig. 8: 3kW bridgeless totem-pole PFC hardware prototype featured by ICERGi controller IC70101 and 8 x isolated gate drivers IC70101.

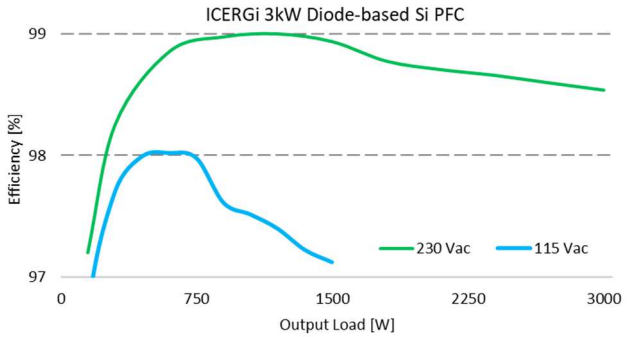

Fig. 9: 3kW diode-based PFC reference design efficiency data with input voltage $V_{IN} = 115V_{AC}$ and $230V_{AC}$ (33kHz operation up to 50% output load)

TABLE I. 3kW Diode-based PFC Bill of Materials (BOM)

Component	*Name*	*Description*	*Qty*
Output capacitors	C_{Out}	470µF 450V electrolytic	3
Flying capacitors	C_{Fly}	3.9µF 450V film	2
Main PFC Inductor	L_{Main}	500µH (2 x 125µ cores)	1
HF MOSFETs	$Q_{1\text{-}8}$	150V 9mΩ BSC093N15NS5	8
Bridge Rectifier	D_{DB}	25A 800V (BU2508)	1
EMI Input Filter	---	1µF 310V_{AC} X – capacitors 3.5mH CM chokes (1.3mm) 470pF 310V_{AC} Y – capacitors	1 2 4

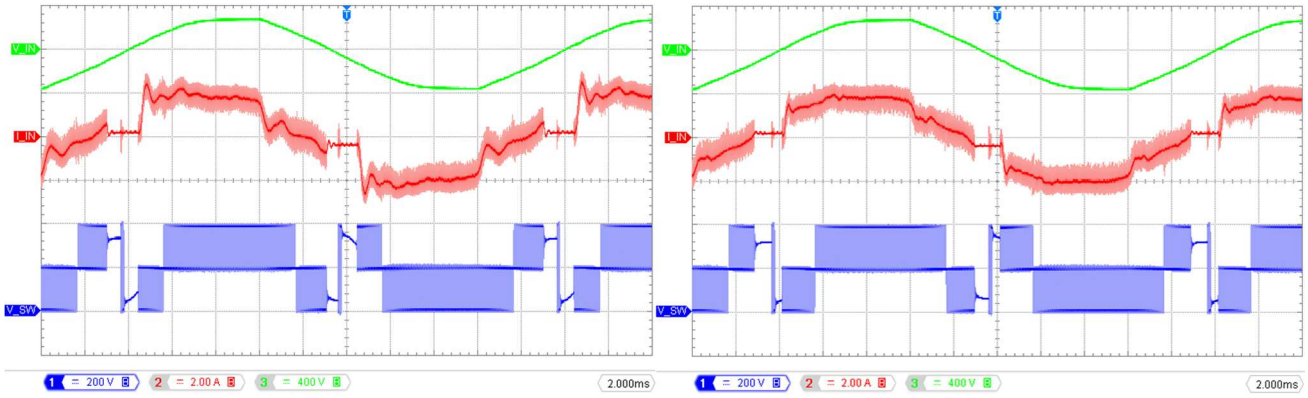

Fig. 10: Steady state waveforms without (left) and with (right) switched gain current sense amplifier arrangement at switching frequency f_{SW} = 33kHz. Switch node (BLUE), input current I_{IN} = 1.3A_{RMS} (RED), input voltage V_{IN} = 230V_{AC} (GREEN).

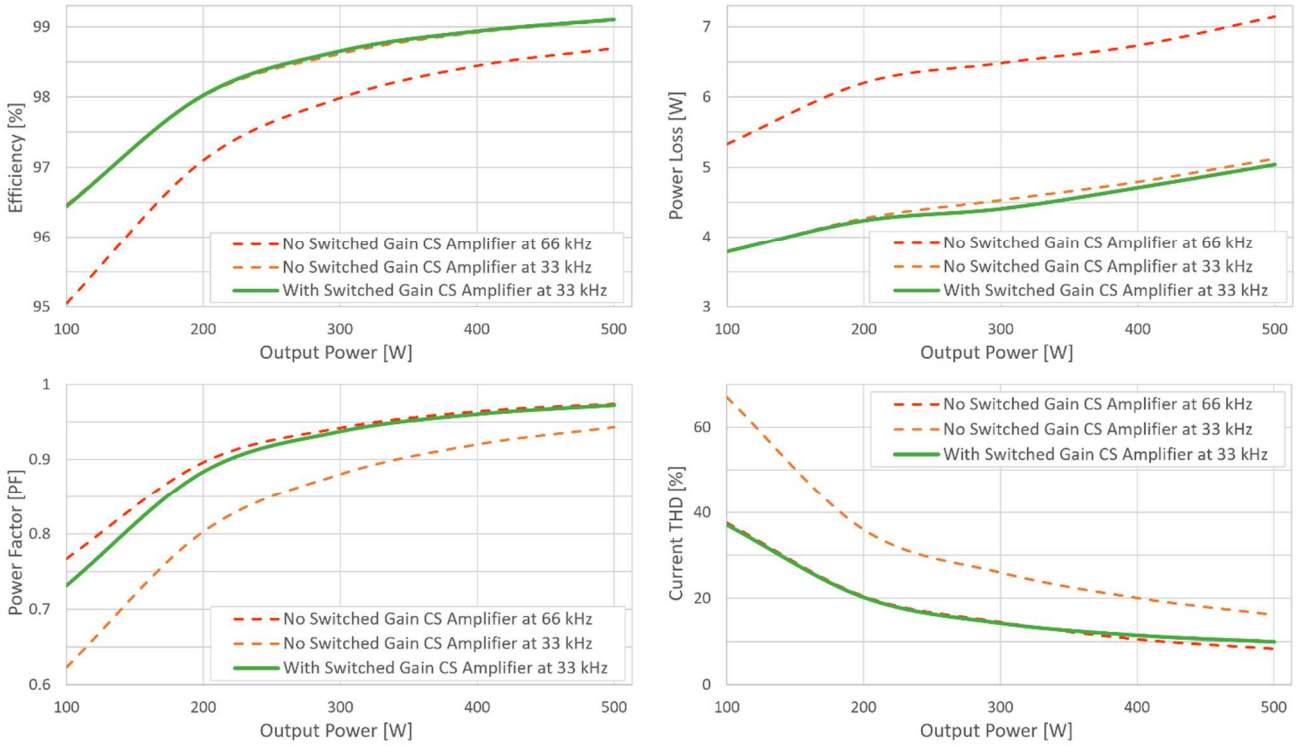

Fig. 11: Experimental measurement results of a 3kW diode-based PFC prototype captured with input voltage V_{IN} = 230$V_{AC.}$ Converter efficiency (top left), total power loss (top right), power factor (bottom left), input current THD (bottom right). Test results are obtained from a synchronous 3kW PFC converter.

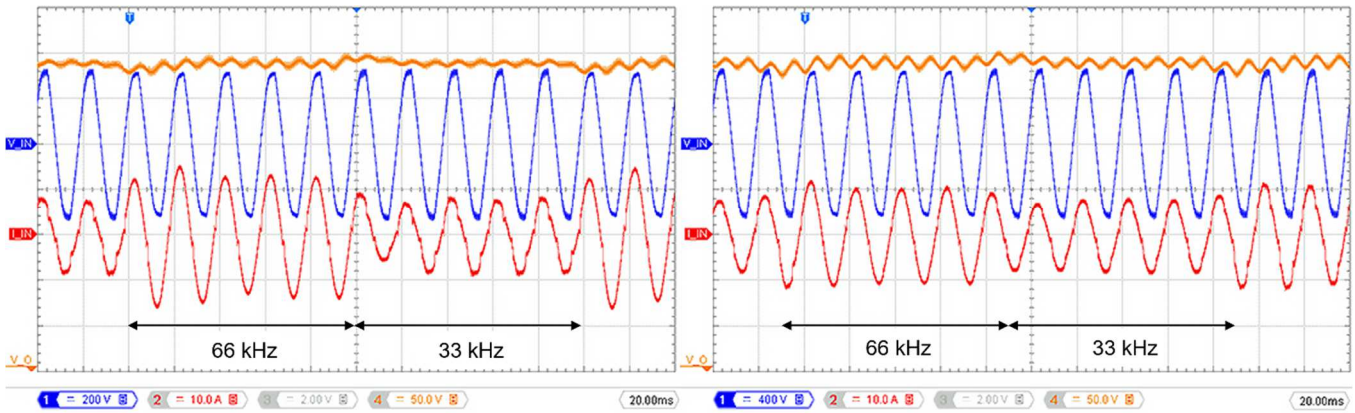

Fig. 12: Transient waveforms with an alternating step load of 400W (ramp up/down of 4A/60µs) captured at low-line V_{IN} = 115V_{AC}, V_{OUT} = 390V_{DC}, P_{OUT} = 700W – 1100W (left) and high-line V_{IN} = 230V_{AC}, V_{OUT} = 390V_{DC}, P_{OUT} = 1400W – 1800W (right). The pulse width between each step load values is 100ms.

For accurate comparison, in both scenarios the converter is operated with 33 kHz switching frequency at 300W output load and an input voltage of $230V_{RMS}$. Fig. 10 illustrates the corresponding waveforms with and without a switched current sense amplifier using 10 mΩ and 5 mΩ current sense resistors, respectively. The effectiveness of the proposed solution is depicted in Fig. 11 above. All the measurements are obtained using a set of Tektronix PA1000 power analyzers. For a given output power range up to 500W, the proposed switching frequency control method allows for power loss saving of around 2W on average. Moreover, it does not undermine the input current THD, and power factor as compared with the former design utilizing a switching frequency of 66 kHz. Even though the power loss associated with the shunt resistor is doubled, considering the worst-case scenario with a maximum input current of 13.5_{ARMS}, increased power loss due to R_{CS} corresponds only to around 0.06% with $V_{IN} = 115V_{AC}$ at $P_{OUT} = 1500W$ and 0.03% with $V_{IN} = 230V_{AC}$ at $P_{OUT} = 3000W$.

VI. Conclusion

In this paper, a practical switching frequency control to reduce losses in hard-switched boost PFC applications at light load is presented. By applying the proposed control method, the front-end converter can benefit greatly from a significant improvement in boosted efficiency without compromising the ATHD and power factor. The improvement of the light to medium load efficiency allows to achieve diode-based totem-pole PFC with peak efficiency η_{peak} >99% at $230V_{AC}$ and >98% at $115V_{AC}$. The solution is not limited to a single application and can be adopted in a variety of different hard-switched applications ranging from 700W – 5.5kW.

Some of the technology aspects as well as the implementation details covered in this papers may be subject of patent applications.

References

[1] J. Hu, W. Xiao, B. Zhang, D. Qiu and C. N. M. Ho, "A Single Phase Hybrid Interleaved Parallel Boost PFC Converter," IEEE, Portland, OR, USA, 2018

[2] G. Anand and S. S. K. Singh, "Design of single stage integrated bridgeless-boost PFC converter," IEEE, Greater Noida, India, 2014

[3] T. T. Vu and E. Mickus, "99% Efficiency 3-Level Bridgeless Totem-pole PFC Implementation with Low-voltage Silicon at Low Cost," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019

[4] "Clearesult," 2021. [Online]. Available: https://www.clearesult.com/80plus. [Accessed 20 07 2021]

[5] "Cybenetics," [Online]. Available: https://www.cybenetics.com/index.php?option=eta_9-51-40. [Accessed 2021 07 22]

[6] Q. Li, F. C. Lee, M. Xu and C. Wang, "Light Load Efficiency Improvement for PFC," IEEE, San Jose, CA, USA, 2009

[7] Z. Ye and B. Sun, "PFC efficency improvement and THD reduction at light loads with ZVS and valley switching," IEEE, Orlando, FL, USA, 2012

[8] T. T. Vu and R. Beinarys, "Feasibility Study of Compact High-efficiency Bidirectional 3-Level Bridgeless Totem-pole PFC/Inverter at Low Cost," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, USA, 2020

[9] R. Beinarys and T. T. Vu "Hybrid Voltage Balancing Control in 3-level Bridgeless Totem-pole PFC," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021