Multilevel Technologies
The "Next Step" After Interleaving Approaches

1. Background

INTERLEAVING APPROACHES are well recognised as having benefits in power factor correction ("PFC") at mid – high power levels. Being able to share the thermal load between separate MOSFETs, diodes and magnetics all helps, as does the ripple reduction associated with cancellation of ripple currents due to phase offsets. Effectively, interleaving places typically two or three complete lower-power converters in parallel. Voltage stresses are similar, and two or three magnetic elements are needed.

MULTILEVEL APPROACHES take this "sharing" approach also, and implement it by stacking conversion cells on top of one another. This technology is well proven and has been used widely in railway systems and other critical high-voltage systems. It has also been introduced by SolarEdge™ and Huawei™ in mass-market DC-AC inverter systems with several kW rating. The ICERGi® technology allowing its cost-effective usage for "conventional" single-phase 400V Power Factor Correction in AC-DC conversion has recently come available, and this gives considerable advantages. Fig. 1 below shows the interleaved (left) and multilevel (right) converter structure.

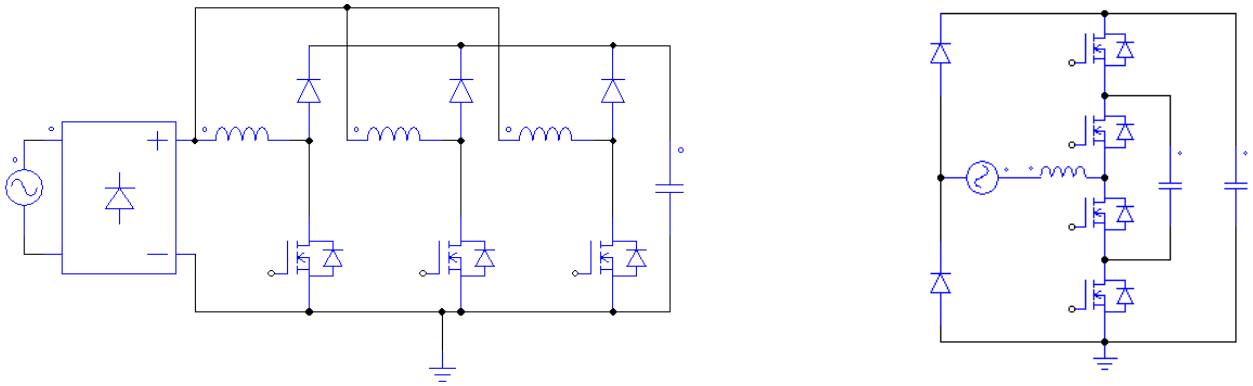

Fig. 1 Showing parallel nature of interleaved PFC (left) and stacked nature of Multilevel Approach

2. Multilevel Technology

MAGNETICS VOLUME – The PFC inductor voltage ripple (measured in Volt-seconds – Vs) caused by the switching action imposes design constraints – larger Vs requires a larger inductor. A conventional interleaved converter operating at perhaps 110KHz results in 900Vμs across each of three inductors! This as compared to a 4-cell (5-level) converter operating at 70KHz resulting in a net maximum of 175Vμs across a single required inductor. Specifically, magnetics volume and cost are reduced greatly as a single inductor of ~60μH (which can

be a low-cost toroid) can give equivalent ripple performance to an interleaved design that requires three PQ26 large ferrite inductors. This is illustrated in Fig. 2 below. In practice a 3-level solution may offer the optimal tradeoff between inductor size and flying capacitor cost.

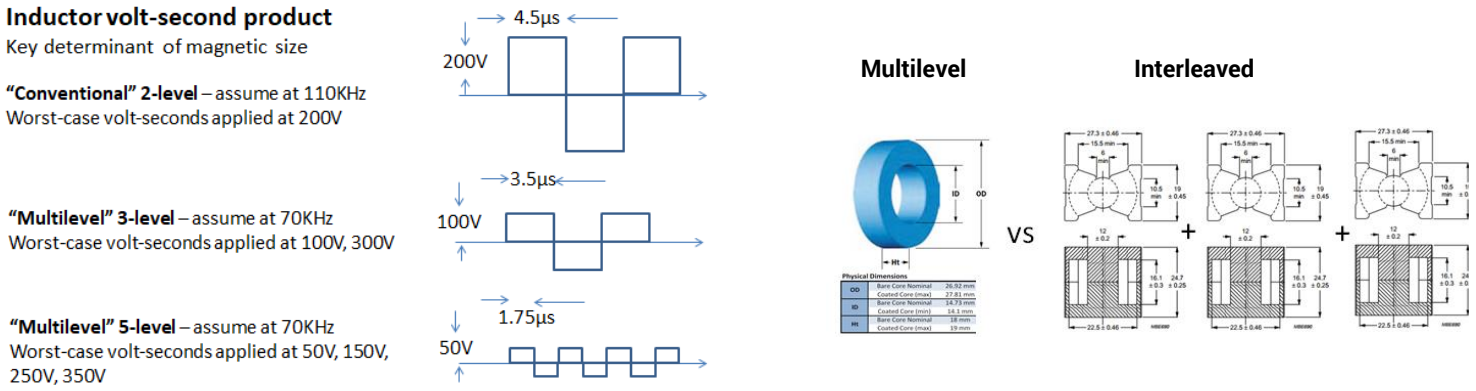

Fig. 2 Showing Magnetic Stress – volt-seconds (left) and size (right) reduction with Multilevel Approaches

SWITCHING EFFICIENCY – In a multilevel converter, switching takes place at the cell level. This means switching at 100V or 200V in each cell, rather than the 400V switching inherent in the parallel operation of converters in Interleaved operation. Losses are associated with $0.5CV^2$ terms as well as V-I overlap, all of which effects are reduced greatly in multilevel conversion, operating directly and/or with switching support devices.

TOTEM-POLE COMPATIBILITY – saving a "Diode Drop". It is well known that the "totem pole" approach represents a preferred "bridgeless" topology, implying that the line current passes through only one rectification element rather than the two diodes as associated with usage of the conventional bridge rectifier. It needs only one inductor and is compatible with synchronous rectification or thyristor-type inrush-control approaches. The totem-pole approach is unsuited to usage with conventional high-voltage MOSFETs due to constraints deriving from body-diode reverse recovery issues. With a multilevel approach, lower voltage FETs with greatly-reduced reverse recovery effects are used, allowing this topology to be used advantageously, with proprietary dIdt control circuitry further supporting low-loss switching.

A key attraction is that 99% efficiency with these topologies can be achieved using standard-format silicon devices, without reliance on GaN or SiC devices.

OVERALL EFFICIENCY – Overall PFC-stage efficiency figures with diode/thyristor usage (including filtering components) can approach 99% at high-line (230V) and exceed 97% at low-line (115V), with synchronous rectification leading to 0.3% and 0.6% higher efficiency figures respectively. This is all achieved in a compact 700W End-End reference design in a 3"x5" format as illustrated in Fig. 3. Figure 4 shows results for a 3kW PFC implementation using a full-bridge totem-pole topology with a 3-level approach, achieving >99% peak efficiency at 230V and >98% at 115V.

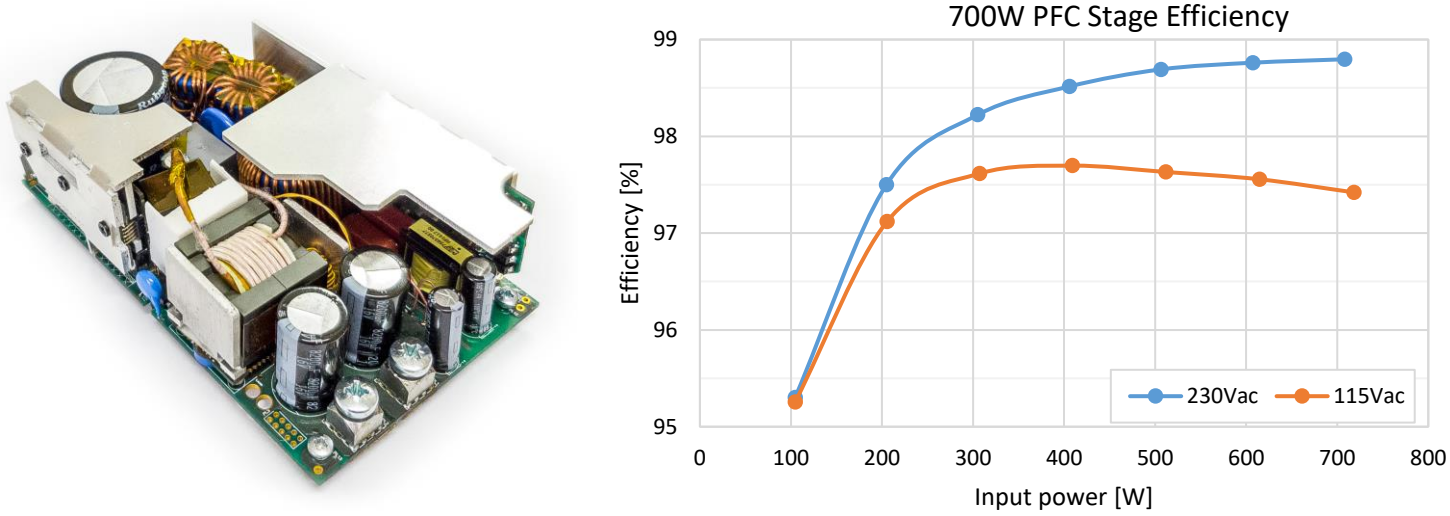

Fig. 3 700W full converter in 3"x5" footprint (left); 700W PFC stage efficiency (right);

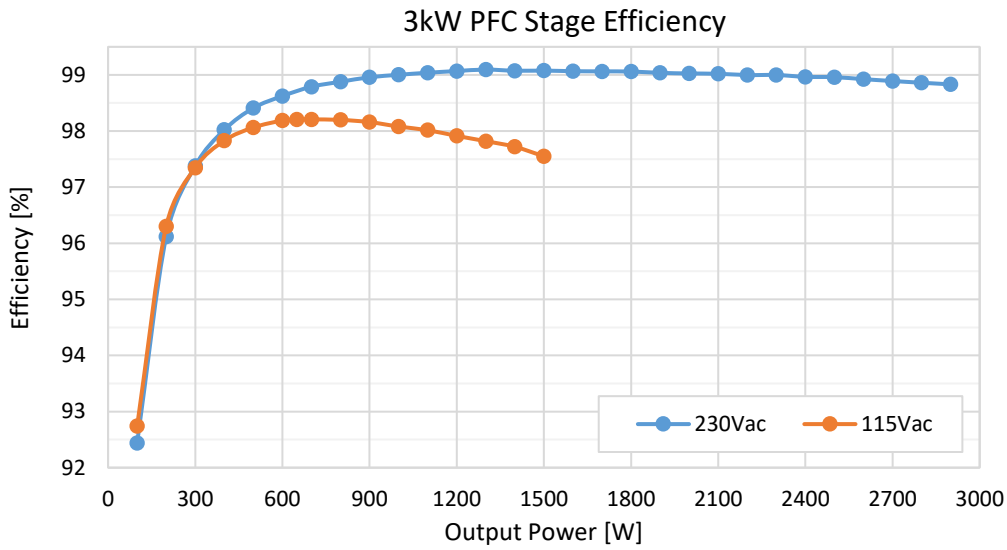

Fig. 4 "Extreme Efficiency" Full-Bridge Totem 3kW PFC-stage efficiency

3. About ICERGi

ICERGi has proved out multilevel technology, combined with digital control, across power levels from several hundred watts up to 3kW, developing low-cost, practical and high-efficiency solutions, with several patented concepts. ICERGi believes it can generate significant value capture as multilevel technology gains traction in AC-DC and DC-AC power conversion. ICERGi products and IP include digital controllers implemented as well as interface drives between controllers and MOSFETs, as well as enhancements to performance and robustness of multilevel topologies.