Minimising Physical Volume in Power Conversion

1. Backdrop

The typical requirement for a power converter is that it take up minimal physical volume in a system, along of course with other requirements in terms of reliability, cost etc.

The physical volume of the active devices – principally the switching semiconductor devices – tends to be miniscule as compared with the physical volume of heatsinks and of passive components. Reducing the physical volume of power conversion circuitry thus involves a focus on each of these areas, and coming up with design approaches that allow miniaturisation of the overall power conversion functionality.

2. Addressing the "Space Users"

The physical volume in power conversion is largely driven by heatsinking, electrolytic capacitors, power inductors (as used in power factor correction and in the output of buck stages) and by EMI filters. A careful focus on each of these areas is essential if compact power conversion functionality is to be achieved.

2.1 Heatsinking

Removal of heat from power converters usually needs the large finned assemblies that are heatsinks, as well as in many cases air movement devices that are needed to cool the power converter. Very large volume savings are possible here, often with the bonus of allowing natural convection as an alternative to forced-air cooling, if losses can be halved. This comes down often to a cost vs volume tradeoff, with "extreme" approaches such as using active switches in all positions in power factor correction or in unfolding bridges in inverter systems getting increasingly justified as semiconductor functional vs cost improves.

So – in designing for small physical volume in real deployments, high efficiency is the most important attribute. One achieves high efficiency by using:

- Power factor correction approaches with minimal conduction losses and minimal switching losses.
- Resonant-type isolation stages that again minimise switching and conduction losses, using synchronous rectification with efficient control.

The systems benefits of generating minimal heat are of course well recognised, in terms of energy cost and in yielding a range of operational performance improvement that can translate to improved reliability from lower operating temperatures and/or reduced cost of heatsinking and thermal management devices.

2.2 Electrolytic Capacitance

Electrolytic capacitors are usually required to store energy consistent with holdup and ride-through requirements under line dropout conditions of between 10ms and 20ms. The physical volume of electrolytic capacitors – assuming parity as to voltage rating, lifetime and ripple current ratings – is directly related to energy storage, or to capacitance given that energy storage is $0.5CV^2$, where C is the capacitance value and V is the applied voltage.

Reducing the size of electrolytic capacitors at a given voltage rating thus implies a reduction in the capacitance value, with consequences that need to be managed as follows:

Ripple voltage will increase at a given power level as the capacitance value is reduced. With a typical analog controller, this easily is translated into distortion of the current waveform.

Digital control techniques – either using a comb-filter approach or using a discrete control approach which guarantees a constant Re during the subsequent half cycle. R_e in this case is the emulated resistance. In Power Factor Correction one desires that instantaneous V and I values are related linearly, such that $V=R_eI$. The digital control approach also needs to adjust for sudden load transients, managing the deviation in bulk capacitor voltage under such conditions.

The practicality of using a smaller value of bulk electrolytic capacitance is also influenced greatly by the design of the downstream stage.

Typically, the downstream stage is designed for correct operation over a voltage range of perhaps 300V to 420V. Designing for a wider range causes loss of efficiency in forward-type converters such as the phase-shifted full bridge topology. Typically, maximum duty cycle corresponds to the dropout level, and operation under normal conditions at ~400V is then associated with reduced duty cycle and higher RMS currents. Design of an LLC converter to operate with progressively high boosting ratios results in reduced efficiency due to increased circulating currents, and challenges associated with control under such conditions.

This aspect has been well recognised, with dual-mode approaches implemented in various ways. The attraction of a dual-mode approach is that one can have a reduced range for the normal mode of operation – typically 330V-420V – associated with near-optimal efficiency. An auxiliary mode can then operate so as to allow continued operation down to perhaps 170V. In going from 400V -> 300V one has used $(1-(¾)^2)$ or 7/16 (44%) of the available energy in the electrolytic capacitor, whereas if the operating range is from 400V to 170V one uses 82% of the available energy. Using an approach that allows operation down to 170V can thus allow a near-halving of the capacitance value and physical volume requirement.

The approach adopted by ICERGi involves putting a multilevel resonant converter into a high-gain mode as bulk capacitor voltage drops. This is so as to maintain output voltage as the output voltage is reduced in this fashion down to approximately 170V.

This implies capacitance value choices for 200W of 68uF and for 1KW a value of 330uF, less than 50% of what typically would be used at these power levels.

Advanced control approaches as cited maintain suitably sinusoidal current waveforms in spite of usage of small values of energy storage capacitance.

2.3 Power Inductors

Power inductor volumes are typically proportional to the energy storage capability of $0.5LI^2$. If we elect to operate with low AC-ripple, then the I value here is effective the line current, which will not vary with topology. One is thus looking to minimise the L value consistent with low ripple.

Multilevel topologies facilitate very significant reduction in inductor size – and as ripple currents can be made very small, then AC-associated losses in windings and core material can also be reduced materially. The basis of operation here is that peak-peak voltage as applied to the inductor is reduced by a factor of three in a three-cell multilevel converter as compared with a standard converter, and the frequency of applied voltage is also increased by three – thus giving an effective nine-times reduction in demands on a power factor inductor, for example. This can result in a smaller core, also with reduced loss, and/or material reduction in size of the EMI filter. Such approaches also lead to opportunities for greatly reduced values of power inductance in other deployment areas in power electronics – such as in filtering for outputs from inverters operating at line frequencies or in digital audio applications, or in filtering of the interface to a capacitor bank operating in buck-boost mode in a shunt active filter usage.

2.4 EMI Filters

EMI filters can take up a significant volume in power converters, and good design of power converters – effectively stopping EMI at source – is consistent with reducing the size of such circuit blocks.

EMI management really has three aspects, treated as follows:

- Differential Mode Conducted – at frequencies up to 30MHz – really managed by having low ripple current in boost inductors, along with pi-filter sections. High-density, high-efficiency design frequently requires separate common-mode and differential-mode inductances, as the leakage inductance of small-turns-count common-mode chokes can be insufficient for material differential-mode filtering. Having a fundamental component at 3x the switching frequency allows a smaller filter to be designed, with usage of smearing giving additional design margin relative to requirements.
- Common-mode Conducted – at frequencies up to 30MHz – really managed by careful transformer design with shielding such as to balance voltages across the isolation gap and along the width of the winding such that minimal current is caused to flow in Y-capacitances. Careful design can reduce the size f common-mode filtering elements.
- Radiated EMI, at frequencies above 30MHz. This is best eliminated at source through usage of very small loop area for switching nodes and associated circuitry. Multilevel structures in PFC stages with a cellular design approach can allow very “tight” placement of surface-mount switches with associated ceramic capacitors, and usage of resonant approaches for isolation stages is also conducive to low radiated emissions.

These approaches can thus be used as part of an overall design approach that can yield cost-effective and efficient designs.

3. Summary

Power conversion is increasing being seen as “adiabatic” in a systems context i.e. – happening without material thermal impact. This goal may well come close to being realised in DCDC conversion at low voltages, where highly-efficient buck converters at low voltage can dissipate minimal amounts of power in comparison to the adjacent processor devices on a circuit card. At the ACDC level, however, power conversion is the sole function of the circuit assembly, and hence a focus on size and efficiency is important.

A focused approach as outlined here can thus reduce size materially in ACDC power conversion.