Implementation of Multi-level Bridgeless PFC Rectifiers for Mid-Power Single Phase Applications

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***Abstract*— Multi-level approaches to AC/DC power conversion have been successfully deployed in high-voltage high-power industrial applications, and are recently considered for mid-power ranges due to their capability of reducing component sizes and improving efficiency. The main challenge for mid-power deployment is the complexity of sensing circuits and control algorithms used to maintain the capacitor voltage balance, which typically results in expensive and impractical designs. Although several studies have been carried out to address the issue, they have not simplified the system complexity and fully exploited the advantages of multi-level converters. This paper presents a new four-level topology for PFC rectifiers, and demonstrates its performance and practicality through a 200W prototype. The theoretical works and experimental results are also provided to confirm the feasibility of the solution.**

Keywords— PFC; multi-cell conversion; bridgeless rectifiers; voltage balancing

I. INTRODUCTION

In offline switched mode power supplies, the conversion from alternative current (AC) to direct current (DC) was conventionally performed by means of a half-wave or full-wave rectifier followed by a storage capacitor. The combination of these components forms nonlinear impedance seen from the mains, which distorts the current drawn from the power supply input and, in turn, pollutes the AC mains with rich harmonic content. Since only the fundamental component contributes to real power flowing into the power supply, the presence of high frequency and high magnitude harmonics is not desirable, and, according to IEC 61000-3-2 [1], should be limited for applications with input power above 75W in general, and lighting applications with a lower threshold in particular. Therefore, power factor correction (PFC) becomes a universal requirement in such contexts.

Driven by market demand for smaller and greener power supplies, there is considerable attraction in being able to reduce the size of the PFC choke and EMI filter which can account for 30% plus of the volume utilization. Two well-known solutions are to either interleave several boost converters [2] or rely on multi-cell topologies [3] – [5]. Although they both allow inductor volume reduction through current ripple cancelation, multi-cell power conversion is much more advantageous in terms of efficiency, EMI filters and device stresses, and, as a result, is mainly considered in the development of a new PFC approach.

Multilevel conversion techniques have been widely adopted in high voltage and high power DC-to-AC inverters and DC-to-DC choppers, where a single switching device either is unable to handle a significant voltage swing, for example over 5kV, or cannot provide adequate performance in terms of speed, efficiency and electro-magnetic interference (EMI). The key purposes of multilevel approaches are to use multiple switches for evenly sharing the voltage stress, which allows the deployment of lower voltage rating but faster switching devices.

Recently, several studies were dedicated to development of universal PFC rectifiers using multilevel approaches [2] – [4]; however, they either borrow the same setup aimed for high voltage and high power applications [2], limit themselves to three levels only [3, 4], or require a dedicated downstream stage to balance capacitor voltages [5]. There is no PFC study that fully takes advantages of multilevel approaches, i.e. deployment of low voltage MOSFETs for applications with universal input voltage, and simplifies the control complexity associated with inherent voltage balancing issues. Therefore, this paper focuses on developments of a new four-level bridgeless PFC topology that is able to overcome all these cited limitations.

II. GENESIS OF THE NEW MULTI-LEVEL BRIDGELESS PFC RECTIFIER

Minimizing conduction losses for the PFC rectifier is desirable in the context of power supplies, and this topic has been intensively discussed in various studies [6] – [11]. Among the proposed solutions, the totem pole bridgeless topology is the most attractive one due to its simplicity and low conduction losses [6], [9] – [11]. Despite all these features, the totem pole bridgeless approach is not particularly welcomed in practice. The main setbacks come from poor reverse-recovery performance of the body diodes of the high voltage MOSFETs operating in continuous conduction mode (CCM), and the complication in control design and gate drive circuitry.

Given the fact that the reverse recovery issues are more relevant to high voltage MOSFETs than to lower voltage rating ones, the hard switching challenges associated with the totem pole arrangement can be elegantly addressed by exploiting multilevel conversion techniques [3]. In particular, the two-switching-device totem pole leg is replaced by a four level flying capacitor multilevel converter stage as illustrated

in Fig. 1. Flying capacitors are chosen instead of other multi-cell topologies because (a) a least number of switches is required for implementation, (b) voltage balance comes naturally for a given modulation scheme, and (c) output harmonic spectrum is theoretically reduced by 4 times as compared to a conventional totem pole approach.

In addition to the use of multiple switches, two thyristors T_1 and T_2 as shown in Fig. 1 are also used in the position of rectifier diodes, allowing ease of inrush current management and startup. In order to prevent inrush current from going through the inductor L and MOSFET string on startup, two bypass diodes D_1 and D_2 are provided to allow an alternating path to the bulk capacitor C_{bulk}.

The inductor L, MOSFET string, and flying capacitors C_{lv} and C_{lh} form a 4-level synchronous boost converter. However, unlike existing multi-level topologies, the flying capacitor voltages v_{hv} and v_{lv} can be initialized and forced to return to their balanced levels during transient responses by a passive clamped circuit enclosed by the dashed line in Fig. 1.

The proposed circuit as shown in Fig. 1 inherits the operating principle of the original totem pole arrangement. Particularly, in the positive half line-cycle, where T_2 is conducted and T_1 is off, the converter operates in a similar fashion as synchronous boost converters with MOSFETs Q_4, Q_5, and Q_6 operating as boost switches while the reverse conduction characteristics of MOSFETs Q_1, Q_2, and Q_3 serve as rectifiers feeding the bulk capacitor C_{bulk}. The operation in the opposing half line-cycle is also similar to synchronous boost converters; however, those MOSFETs swap their roles and the inductor current flows in an inverse direction.

The interactions between the multi-level boost converter and the diode clamped circuitry are quite complex; therefore, for ease of interpretation, the operation of each sub circuit is presented separately in Sections III and IV.

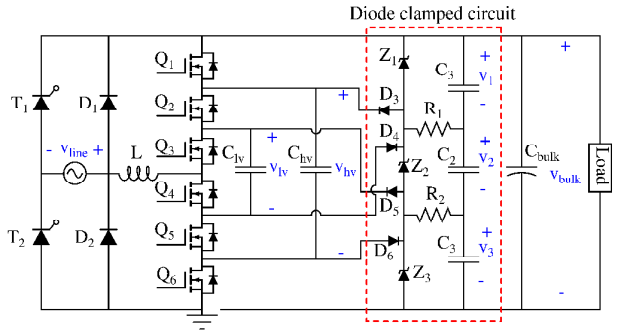

Fig. 1: Proposed 4-level bridgeless totem pole boost rectifier with balance enforcement circuitry

III. FOUR-LEVEL SYNCHRONOUS BOOST CONVERTER

A. *Operating principle*

Due to the symmetry of the proposed rectifier, only positive half-line cycles are considered here for simplicity, and the thyristor T_2 is assumed to be conducted while T_1, D_1 and D_2 are off. Without the balance enforcement mechanism, the circuit as shown in Fig. 1 can be simplified to a four-level boost converter which is illustrated in Fig. 2.

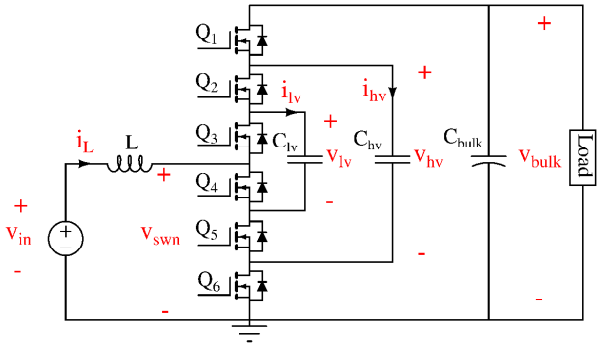

Fig. 2: Four-level flying capacitor boost converter

The operation of six MOSFETs in the string can be summarized as follow. Firstly, the switching devices are split into 3 pairs of switches including (Q_1, Q_6), (Q_2, Q_5), and (Q_3, Q_4). Each arrangement of paired switches is operated in a complementary manner, i.e. when one switch of the pair is on, the other must be off and vice versa. The control signals for the three top switches Q_1, Q_2 and Q_3 share the same duty ratio D and the switching frequency f_{pwm}, but are different in phase by an angle of 120 degrees while Q_6, Q_5 and Q_4 are driven by negating the driving pulses of Q_1, Q_2 and Q_3, respectively.

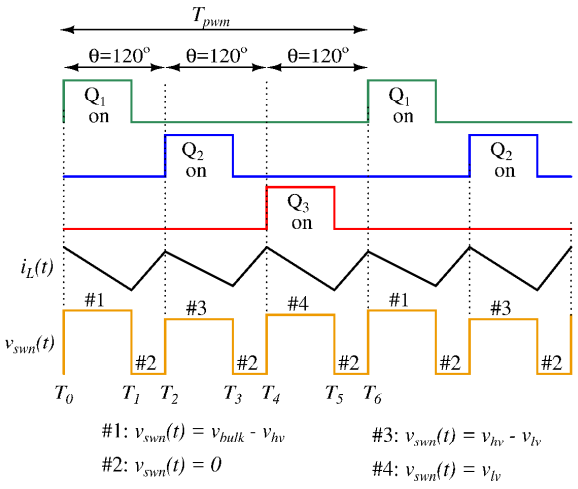

Fig. 3: Operational waveforms of a four-level synchronous boost converter with $0 < D \leq 1/3$

Since a phase shift of 120 degrees is equivalent to a time shift of one third of the switching period, the four-level boost converter changes its switching sequence every time D crossing the 1/3 and 2/3 points, which is illustrated in Fig. 3, Fig. 4 and Fig. 5, respectively. In particular, each number going with a hash symbol in those figures represents a unique combination of the states of Q_1, Q_2 and Q_3, and a unique relationship between the switched node voltage $v_{swn}(t)$, the flying capacitor voltages and the output voltage. If we consider the duty ratio range of (0 1/3] as shown in Fig. 3 as an

example, the switching sequence within a switching cycle is #1, #2, #3, #2, #4, #2, and this order is preserved over the next cycles.

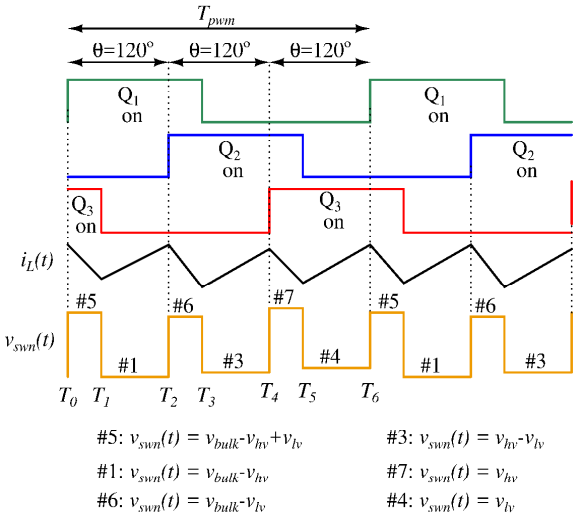

Fig. 4: Operational waveform of a four-level synchronous boost converter with $1/3 \le D \le 2/3$

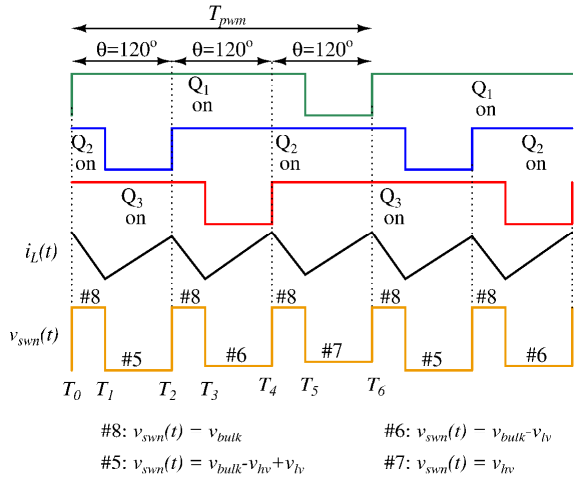

Fig. 5: Operational waveforms of a four-level synchronous boost converter with $2/3 \le D < 1$

Deriving the steady state responses for three operating modes of the multi-level boost converter can be carried out in a similar manner; therefore, for simplicity, Sections III.B and III.C focus on the analysis for D between 0 and 1/3 only, and summarize the final results for other cases.

B. DC analysis

The converter is assumed to operate in continuous conduction mode (CCM), and have negligible voltage ripples across the capacitors. The inductor current and switched node voltage waveforms are illustrated in Fig. 3: Operational waveforms of a four-level synchronous boost converter with $0 < D \le 1/3$. Applying the voltage-second balance principle to the inductor gives

$$\sum_{i=0}^{5} v_L[i]\Delta T_i = \sum_{i=0}^{5} (v_{in}[i] - v_{swn}[i])\Delta T_i = 0 \qquad (1)$$

where the index i denotes the time interval from the time instant T_i to T_{i+1} and $\Delta T_i = T_{i+1} - T_i$. Substituting the expression of $v_{swn}(t)$ as given in Fig. 3 into (1) gives

$$\sum_{i=0}^{5} v_{line}[i]\Delta T_i - D v_{bulk} = 0 \qquad (2)$$

In most scenarios, the input voltage changes very slowly and can be considered as constant over a switching cycle. This assumption allows simplification of (2) into

$$\frac{V_{bulk}}{V_{in}} = \frac{1}{D} \qquad (3)$$

The net charge accumulated by two flying capacitors over one switching cycle should be also zero at steady state, which means

$$\begin{aligned} \sum_{i=0}^{5} i_{lv}[i]\Delta T_i &= 0, \\ \sum_{i=0}^{5} i_{hv}[i]\Delta T_i &= 0. \end{aligned} \qquad (4)$$

One can verify from Fig. 2 that the capacitors C_{lv} and C_{hv} gets charged and discharged by the inductor current i_L for the same amount of time within each switching cycle. This suggests that the left-hand sides of (4) will be always zero if the assumption of negligible inductor current ripples is applied. Therefore, one needs a better approximation of i_L so as to get more useful information from these equations. One simple solution here is to take account of increments in the inductor current during each subinterval of the switching cycle. Particularly, if the voltage across the inductor during the time interval $[T_i, T_{i+1}]$ is $v_L[i]$, the inductor current during such an interval can be approximated by

$$i_L[i] = I_L + \frac{v_L[i]\Delta T_i}{2L} \qquad (5)$$

where I_L is the averaged inductor current without ripples. Following such a principle allows us to transform (4) into

$$\begin{aligned} V_{bulk} - 2V_{hv} + V_{lv} &= 0, \\ V_{hv} - 2V_{lv} &= 0. \end{aligned} \qquad (6)$$

Solving (6) for V_{lv} and V_{hv} gives

$$\begin{aligned} V_{lv} &= \frac{1}{3} V_{bulk}, \\ V_{hv} &= \frac{2}{3} V_{bulk}. \end{aligned} \qquad (7)$$

where V_{bulk} denotes the DC value of the bulk capacitor voltage. One can easily confirm that (3) and (7) are valid for all operating modes of the converter, i.e. any value of the duty

ratio within the range (0, 1). Given the voltages across the flying capacitor, the operating voltage of all MOSFETs can be approximated by $V_{bulk}/3$ which is technically reduced by a factor of 3 as compared to that of a conventional totem pole arrangement. If the nominal voltage of the bulk capacitor is assumed to be 400V, the nominal operating voltages of switching devices are 133.3V. This allows the usage of 200V MOSFETs which switch much faster and more efficiently than 600V counterparts; hence, conventional switching operation can be exploited here with minimum loss penalty. Another benefit of low voltage MOSFETs is the capability to switch at high frequencies which allows material reduction in the size of the PFC choke.

C. Capacitor voltage and inductor current ripples

Knowing the voltage and current ripples is important in the context of component selection as well as performance comparison. The simplest way is to examine the voltage across the inductor and the currents going through the flying capacitors at steady state. In particular, the DC values of v_{lv} and v_{hv} as described in (7) imply that the switched node voltage $v_{swn}(t)$ as highlighted in Fig. 2 can be well approximated by a periodic square wave having a frequency of three times the switching frequency. Knowing $v_{swn}(t)$ allows derivation of the peak-to-peak current ripples as given by

$$\Delta I_L = \left(\frac{1}{3} - D\right)\frac{DV_{bulk}T_{pwm}}{L}. \qquad (8)$$

Similarly, the ripples of the flying capacitor voltages can be derived by modelling the inductor as a constant current source having a magnitude of

$$I_L = \frac{P_{out}}{DV_{bulk}}, \qquad (9)$$

where P_{out} denotes the load power. Given the switching sequence and timing chain in Fig. 3, the peak-to-peak capacitor voltage ripples can be simply obtained via

$$\Delta V_{lv} = \frac{D^2 T_{pwm} P_{out}}{C_{lv} V_{bulk}}, \quad \Delta V_{hv} = \frac{D^2 T_{pwm} P_{out}}{C_{hv} V_{bulk}}. \qquad (10)$$

For other operating modes of the converter, steady state and ripple analyses can be performed in a similar fashion as discussed in this section. The final results associated with each duty ratio range are collected in TABLE I. As compared to a conventional boost converter, one can see a great similarity in the input-to-output gain but significant differences in the inductor current ripple. Specifically, ΔI_L is suppressed not only at two extreme values of the duty ratio but also at mode transition points, i.e. D = 1/3 and 2/3.

TABLE I: DC GAIN, VOLTAGE AND CURRENT RIPPLES OF THE PROPOSED FOUR-LEVEL TOTEM POLE RECTIFIER

	$0 < D \le \frac{1}{3}$	$\frac{1}{3} \le D \le \frac{2}{3}$	$\frac{2}{3} \le D \le 1$
DC gain V_{bulk}/V_{in}	$\frac{1}{D}$	$\frac{1}{D}$	$\frac{1}{D}$
DC flying capacitor voltage V_{lv}	$V_{bulk}/3$	$V_{bulk}/3$	$V_{bulk}/3$
DC flying capacitor voltage V_{hv}	$2V_{bulk}/3$	$2V_{bulk}/3$	$2V_{bulk}/3$
Inductor current ripple ΔI_L (peak-to-peak)	$\left(\frac{1}{3} - D\right)\frac{V_{in}T_{pwm}}{L}$	$\left(D - \frac{1}{3}\right)\left(\frac{2}{3D} - 1\right)\frac{V_{in}T_{pwm}}{L}$	$\left(1 - \frac{2}{3D}\right)(1 - D)\frac{V_{in}T_{pwm}}{L}$
Flying capacitor voltage ripple ΔV_{lv} (peak-to-peak)	$\frac{DP_{out}T_{pwm}}{V_{in}C_{lv}}$	$\frac{D}{3}\frac{P_{out}T_{pwm}}{V_{in}C_{lv}}$	$(1 - D)\frac{P_{out}T_{pwm}}{V_{in}C_{lv}}$
Flying capacitor voltage ripple ΔV_{hv} (peak-to-peak)	$\frac{DP_{out}T_{pwm}}{V_{in}C_{hv}}$	$\frac{DP_{out}T_{pwm}}{V_{in}C_{hv}}$	$\frac{DP_{out}T_{pwm}}{V_{in}C_{hv}}$

If the PFC output is assumed to be unchanged at steady state, the voltage and current ripples as formulated in TABLE I can be described as functions of D, which allows theoretical derivation of maximums of these quantities, which is summarized in TABLE II.

The results as presented in TABLE II show that the maximum current ripple in the proposed four-level boost converter is one ninth of that of the conventional one. In other words, for the same current ripple, the four-level approach requires nine times less inductance than the conventional

boost converter, or equivalently nine time less stored energy/volume for the same power rating.

TABLE II: MAXIMAL VOLTAGE AND CURRENT RIPPLES

ΔI_L is maximal at $D = \frac{1}{6}, \frac{1}{2}$, and $\frac{5}{6}$	$\frac{1}{36}\frac{V_{out}T_{sw}}{L}$
ΔV_{lv} is maximal at $P_{out\_\max}$ and $V_{in} \le V_{bulk}/3$	$\frac{P_{out\_\max}T_{pwm}}{V_{out}C_{lv}}$
ΔV_{hv} is maximal at $P_{out\_\max}$ and $V_{in} \le V_{bulk}/3$	$\frac{P_{out\_\max}T_{pwm}}{V_{out}C_{hv}}$

IV. FLYING CAPACITOR INITIALIZATION AND VOLTAGE BALANCING

The diode clamped circuit as illustrated in Fig. 1 is proposed to address to two real challenges including capacitor initialization and voltage balancing associated with implementation of a four-level boost converter. In particular, if Z_1, Z_2 and Z_3 are 160V Zener diodes, turning Q1 and Q2 on while keeping other MOSFETs off will activate Z_2 and Z_3, which in turn charges C_{lv} and C_{hv} to $v_{bulk} - 320\text{V}$ and $v_{bulk} - 160\text{V}$, respectively. Therefore, the worst-case voltage stress on the switching devices is 160V which is safe for 200W rating MOSFETs. Two pairs of diodes (D_3, D_4) and (D_5, D_6), current limit resistors R_1 and R_2, and a capacitor array (C_1,C_2,C_3) are provided to supply additional charge to C_{lv} and C_{hv} during the condition where $v_{lv} + v_{hv} \le v_{bulk}$. Although the balance enforcement circuit has no effect when $v_{lv} + v_{hv} > v_{bulk}$, it actually helps to damp/interrupt all disturbances occurring in the flying capacitor voltages due to continual variations in the duty ratio over the line cycle. In order to demonstrate the effectiveness of balance enforcement, a simulation is set up in LTSpice for two operating conditions of the proposed converter, one with balance enforcement and one without such a functionality. The input current is programmed to follow the shape of the input voltage and provide power of 200W to the output. Simulated results for the two test conditions are plotted in Fig. 6 and Fig. 7, respectively.

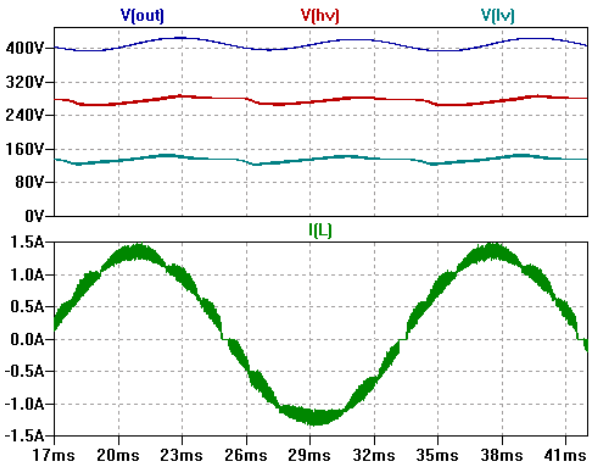

Fig. 6: Capacitor voltage waveforms with balance enforcement. The values of the damping resistance and capacitor string used in the simulation are $R_1 = R_2 = 68\Omega$ and C_1=C_2=C_3 = 100nF.

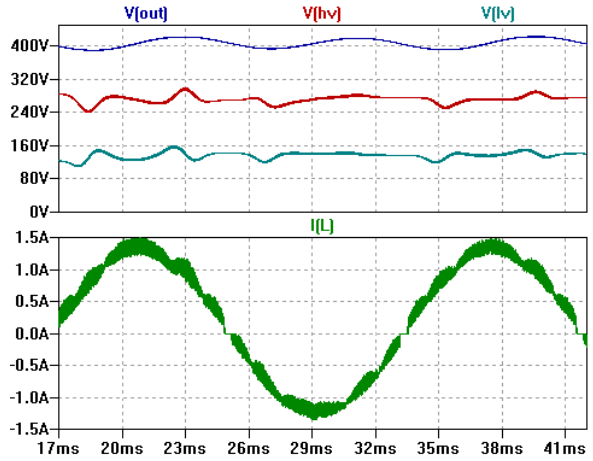

Fig. 7: Capacitor voltage waveforms without balance enforcement

Comparing the data between these figures shows that without balance enforcement, the flying capacitor voltages tend to deviate from the balanced points when the duty ratio command varies, which seems to be unavoidable in PFC applications. One may argue that disturbances in v_{lv} and v_{hv} seems benign, and do not have much effect on the converter operation except slightly distortion in the current waveform as can be seen in Fig. 7. The main concern here is unbalanced voltage stresses on switching devices, which typically gets worse during start-up and step-load transitions Therefore, the role of the clamped circuit is obviously critical in this context.

Although the clamped circuit looks quite complex, it is composed of low-power devices only and, as a consequence, neither take up much real estate from the PCB design nor contribute much to the build of material (BOM) costs.

V. DESIGN AND IMPLEMENTATION

The input data for the design of a four-level converter prototype are listed in TABLE III.

TABLE III: CONVERTER DESIGN SPECIFICATIONS

Input voltage, V_{line}	$85V_{rms}$ - $265V_{rms}$
Bulk capacitor voltage, V_{bulk}	$175V_{DC}$ - $400V_{DC}$
Maximum pk-pk capacitor voltage ripples, ΔV_{lv_max}, ΔV_{hv_max}	10V
Switching frequency, f_{pwm}	150kHz
Maximum output power, P_{out_max}	200W
Efficiency, η	98%
Hold-up time, t_{holdup}	20ms

A. Power stage design

1) Boost inductor selection:

Inductance values are generally determined in an iterative fashion so as to ensure converter operating condition, i.e. continuous or discontinuous conduction mode, component stresses, switching losses and many others. For simplicity, maximal peak current and current ripple are used as a basis for inductor value determination here. If the peak-to-peak current ripple is assumed to be negligible, the maximal peak inductor current can be approximated by

$$I_{pk\_\max} = \frac{\sqrt{2}P_{out\_\max}}{\eta V_{line\_\min}} = \frac{\sqrt{2}*200}{0.98*85} = 3.39\text{A}. \quad (11)$$

Choosing the maximal current ripple of about 5% of I_{pk_max} yields ΔI_{L_max} = 169.5mA. Given the expression of ΔI_L in TABLE II, one can obtain the minimum inductor value via

$$L_{\min} = \frac{V_{bulk}T_{pwm}}{36\Delta I_{L\_\max}} = \frac{400*6.7\bullet 10^{-6}}{36*0.1695} = 437\mu\text{H}. \quad (12)$$

Notice that a 5% ripple specification is actually desirable in the context of EMI filter, core losses and control stability, but is rarely adopted in design of conventional 200W PFC rectifiers as doing this requires a significant large magnetics with an inductance value of as high as 4mH.

2) Flying capacitors determination

The flying capacitors can be calculated from the voltage ripple requirement via

$$C_{hv\_\min} = \frac{P_{out\_\max}T_{pwm}}{V_{bulk}\Delta V_{hv\_\max}} = \frac{200*6.7\bullet 10^{-6}}{400*10} = 333\text{nF},$$
$$C_{lv\_\min} = \frac{P_{out\_\max}T_{pwm}}{V_{bulk}\Delta V_{hv\_\max}} = \frac{200*6.7\bullet 10^{-6}}{400*10} = 333\text{nF}. \quad (13)$$

Considering a margin of 20% for voltage roll off gives C_{lv} = C_{hv} = 1.2*333nF = 400nF.

3) Output capacitor design

Generally, three factors including output voltage ripples, output current ripples, and hold-up requirement are involved in the design of the bulk capacitor. However, in most cases, the hold-up time t_{holdup} is the main factor influencing the size and the value of the bulk capacitor.

Due to the constraints on the input voltage range of conventional downstream stages, the PFC output typically operates between around 300V and 400V, which implies that only 56.25% of the energy storage in the bulk capacitor is recycled for hold-up. For a better use of output capacitance, a stacked multi-phase DC/DC converter with a wide input range [12] is deployed after the PFC stage. The output voltage now can be drained to a value as low as 175V, which suggests minimal bulk capacitance of

$$C_{bulk\_\min} = \frac{2t_{holdup}P_{out\_\max}}{V_{bulk\_nom}^2 - V_{bulk\_\min}^2} = \frac{2*0.02*200}{400^2 - 175^2} = 61.8\mu\text{F}. \quad (14)$$

In this case, a 68μF capacitor can satisfy the minimal capacitance condition with a margin of 10%.

B. Implementation

The design procedure as discussed in Section V.A suggests the following components: C_{bulk} = 68uF – 450V rating-electrolytic, C_{lv} = C_{hv} = 400nF - 450V rating - ceramic, C_1=C_2=C_3 = 100nF - 250V rating- ceramic, and R_1 = R_2 = 68Ω. The PFC choke is implemented by a standard toroid having an outer diameter of 18mm, and an A_L value of 89 nanohenries per turn squared which can provide inductance of 461uH with 72 turns. A roll-off of 60% in the inductance is to be expected at low-line voltage; however, the inductance is over-designed in (12) so it is safe to operate with such configuration The main 200V switches are BSZ900N20NS3G with Drain-Source on-resistance R_{DSon} of 90mΩ, and controlled by ARM Cortex M0 (STM32F051) through proprietary isolated gate-drive circuitry

VI. EXPERIMENTAL RESULTS

Operational waveforms at low line and high line input voltages are illustrated in Figures 3 and 4, respectively. Both experiments are configured to provide a quasi-constant output voltage of 400V. The experimental results show that the converter operates in a stable manner with no sign of voltage imbalance, which confirms the feasibility of the deployment of 200V MOSFETs here. Thanks to the multi-level structure, the inductor current has minimum ripples even no EMI input filter is present during the measurement.

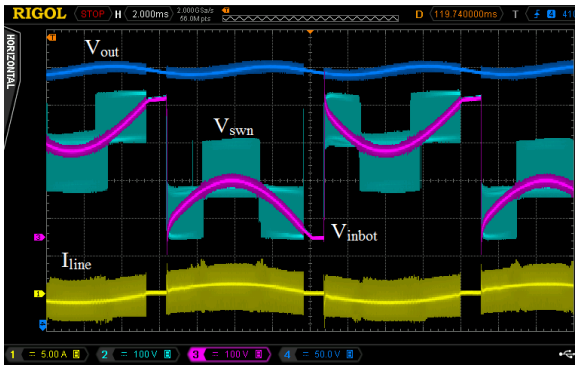

Fig. 8: Operational waveforms of the four-level PFC rectifier at low line input voltage and P_{out} = 100W: (CH1) I_{line} -Input current, (CH2) V_{swn} - Switched node voltage, (CH3) V_{inbot} - Input voltage referred to the bottom, (CH4) V_{bulk} – Bulk capacitor voltage

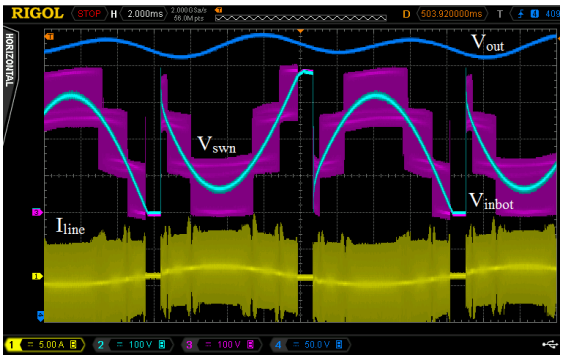

Fig. 9: Operational waveforms of the four-level PFC rectifier at high line input voltage and P_{out} = 200W: (CH1) I_{line} - Input current, (CH2) V_{inbot} - Input voltage, (CH3) V_{swn} - Switched node voltage, referred to the bottom, (CH4) V_{bulk} – Bulk capacitor voltage

VII. Conclusions

This paper presents a commercially-deployed implementation of universal four-level PFC rectifiers using 200V MOSFETs, allowing nine times reduction in the PFC choke, four times reduction in the complete product volume, and materially improvements in the rectifier efficiency and power density. The study also confirms that balancing multi-level flying capacitor converters can be practically and effectively achieved by a passive clamping network, although it is found that cost-effective and low-complexity properties are lost when extending the design to six-level converters or higher. The works also include insight into the theoretical analyses of the four-level synchronous boost converter as well as the balance enforcement mechanism, and discuss the design of the power stage in details.

Some of the technologies and implementation details presented in this paper may be subject of patent applications.

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