How To Design Reliable Multilevel Bridgeless Totem-pole PFC

This article discusses key design guidelines to implement safe operating conditions for power switches, enabling delivery of higher reliability and greater robustness for multilevel totem-pole PFC.

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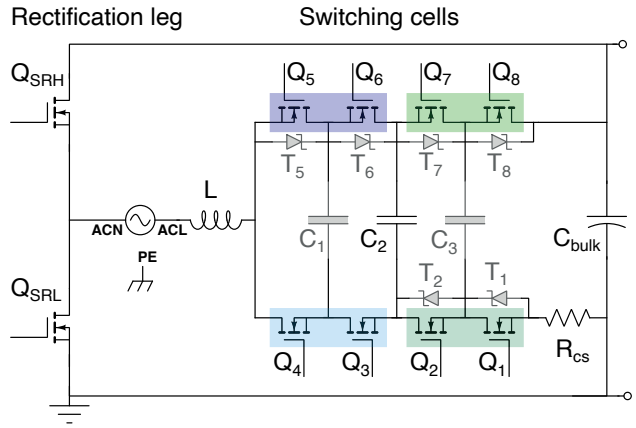
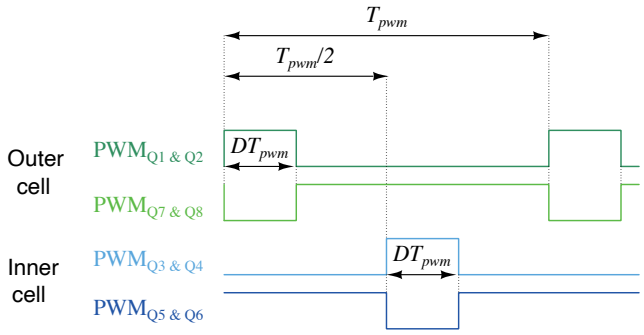
Multilevel totem-pole PFC offers the designer market appealing advantages over 2-level designs including a significantly smaller inductor, much lower dv/dt's and reduced switching losses. The inherent reduction in switch operating voltage enables the multilevel PFC to be optimally implemented by low-cost standard multi-sourced 150V MOSFETs with minimal reverse recovery time and charge. This implementation enables best-in-class efficiency > 99.2% at much lower system cost compared to existing wide-band gap (WBG) solutions in the market.

Multilevel Implementation of Totem-pole PFC



a) Topology



b) Phase-shifted PWM modulation for two switching cells

Figure 1: Bridgeless Totem-pole PFC Design using 150V MOSFETs

Due to the lowest conduction losses, the bridgeless totem-pole arrangement is a preferred PFC topology for single-phase AC/DC applications [1], [2]. The high frequency switching leg can be implemented in either a 2-level fashion using 650V WBG devices [1] or a multi-level arrangement based on readily available 150V MOSFETs [2]. The latter implementation illustrated in Figure 1(a) allows for optimal power conversion with 75% smaller magnetics and 50% lower BOM costs. These substantial benefits are a direct result of how power is digitally modulated and converted from AC to DC. Specifically, 8 x 150V MOSFETs (Q_1 to Q_8) and capacitor C_2 are arranged to form two 2-level switching cells. The inner cell including Q_3, Q_4, Q_5 and Q_6 is controlled to be 180-degrees phase shifted to the outer cell composing of Q_1, Q_2, Q_7, and Q_8. Serially connected MOSFETs in each cell, e.g. Q_3 and Q_4, are driven on and off together by isolated low-cost gate drive circuits based on ICERGi IC70001. Exemplary drive signals for the two switching cells are demonstrated in Figure 1(b).

Since the two switching cells are cascaded and phase-shifted, the multilevel topology processes power more efficiently and quietly than a conventional 2-level solution. In particular, power conversion happens at half of the output voltage and twice the switching frequency of power devices, which results in:

- 4 x reduction in the volt-seconds product for the main inductor. This allows for a 4x smaller inductor design using low-cost standard Sendust toroidal cores and solid enamelled wire, enabling 50% BOM cost reduction. In addition to cost and size benefits, a smaller inductor is more efficient at low-line operation, which improves converter efficiency further.
- Lower switching losses
- Reduced dv/dt which is of value in limiting EMI effects

As similar to any PFC topologies, the reliability of the multilevel totem-pole design is dictated by the life span of power switches, particularly 150V MOSFETs. Therefore, keeping these devices well within their electrically and thermally safe operating areas is required for long life and reliable applications. The next part of the article will discuss how to meet such requirements in a real-word design.

Voltage Balance is Key

Capacitors C_2 and C_{bulk} shown in Figure 1(a) define the operating voltage for each pair of serially connected MOSFETs in a switching cell. However, the operating voltage of each MOSFET may not be well defined depending on its switching characteristics as well as how it is driven [2]. Such sensitivity is fully addressed by adding two flying capacitors C_1 and C_3 to the switching cells as illustrated in Figure 1(a). Maintaining the operating voltage level for all switching devices within their specifications is achieved by controlling the voltage across three flying capacitors C_1, C_2, C_3 and output capacitor C_{bulk}.

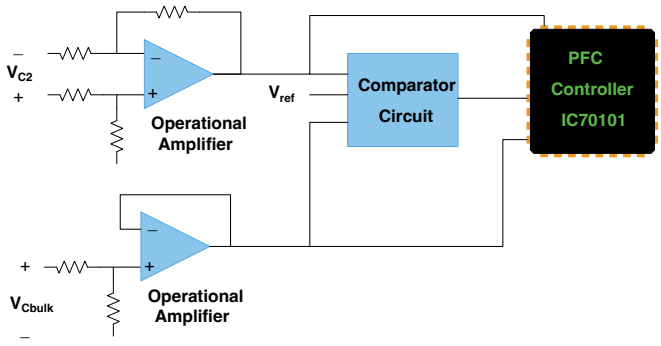
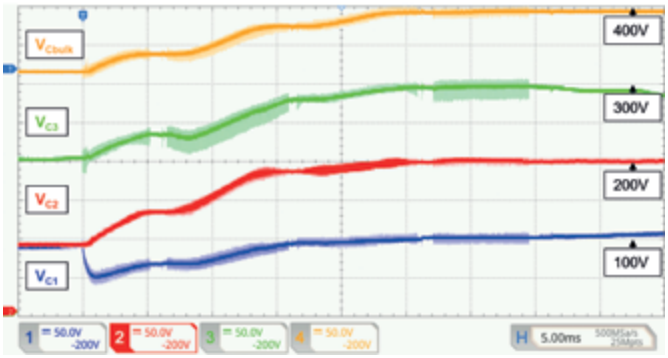


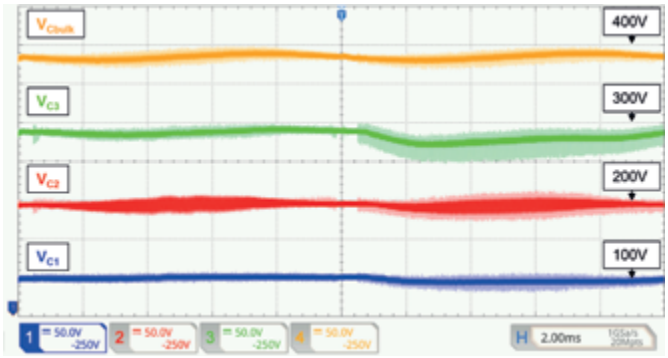
Figure 2: Flying capacitor voltage monitoring and control

The PFC output voltage V_{Cbulk} is measured and regulated by a digital PFC controller. The phase-shifted modulation naturally forces the voltage of C_2 to settle at a half of the output voltage V_{Cbulk}. Even though natural balance is sufficient to address most device and manufacturing tolerances, the flying capacitor voltage V_{C2} should be actively monitored and controlled for greater protection. Such a control feature is incorporated in ICERGi PFC controller IC70101 as illustrated in Figure 2. The voltage across C_2 is first buffered by a differential amplifier whose output is then fed to the PFC controller IC70101 for ADC measurement and software protection. An additional analogue circuitry with fast comparators can be used to provide an extra layer of over voltage protection for switching components.

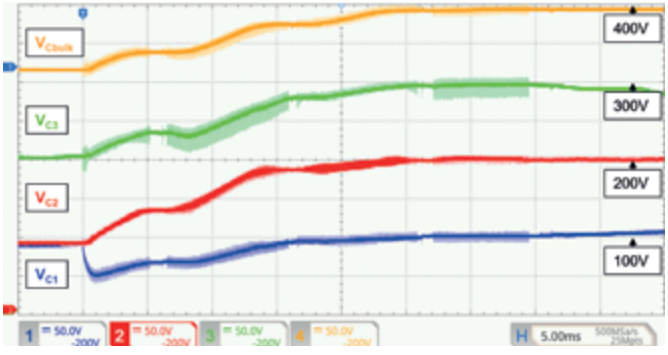
Precise drive delay matching for serially connected MOSFETs is required to minimize the energy absorbed by C_1 and C_3 during turn-off transitions. Such a requirement can be met by using miniature isolated drive transformers in conjunction with ICERGi gate driver IC70001. Since C_1 and C_3 do not have to handle any significant power during operation, their values can be small, e.g. around 47nF. Consequently, their voltage can be effectively controlled by using 4 x TVS devices T_5, T_6, T_7, and T_8. For minimal power losses, the



Start-up: V_{line} = 230V_{ac}, No load



Steady State Operation: V_{line} = 230Vac, P_{load} = 3kW



2kV L-to-N Differential Surge, V_{line} = 230V_{ac}, P_{load} = 2kW

Figure 3: Flying capacitor and output voltage during start-up, steady state, and line voltage surge conditions.
(V_{C1} = BLUE, V_{C2} = RED, V_{C3} = GREEN, V_{Cbulk} = ORANGE)

clamping level is chosen to be above 115V and only triggers one of the TVS devices when V_{C1} and V_{C3} drift away from their balance points of $V_{Cbulk}/4$ and $3*V_{Cbulk}/4$, respectively.

It should be noted that capacitor voltage V_{C2} is well controlled during all operating conditions while the output voltage V_{Cbulk} could experience fast transients during power-up and line voltage surges. Therefore, two additional TVS devices T_1 and T_2 shown in Figure 1(a) are included in the outer cell to provide adequate voltage clamping preventing MOSFETs from entering avalanche mode.

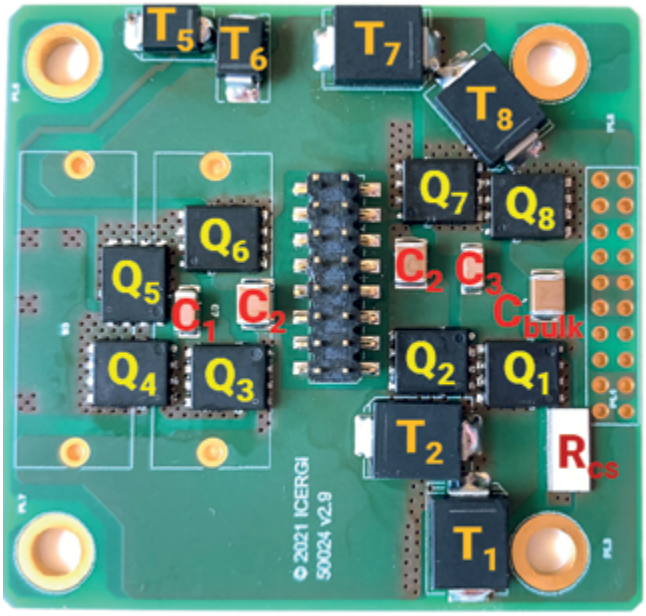


Figure 4: Recommended PCB layout for switching cells of multilevel totem-pole PFC

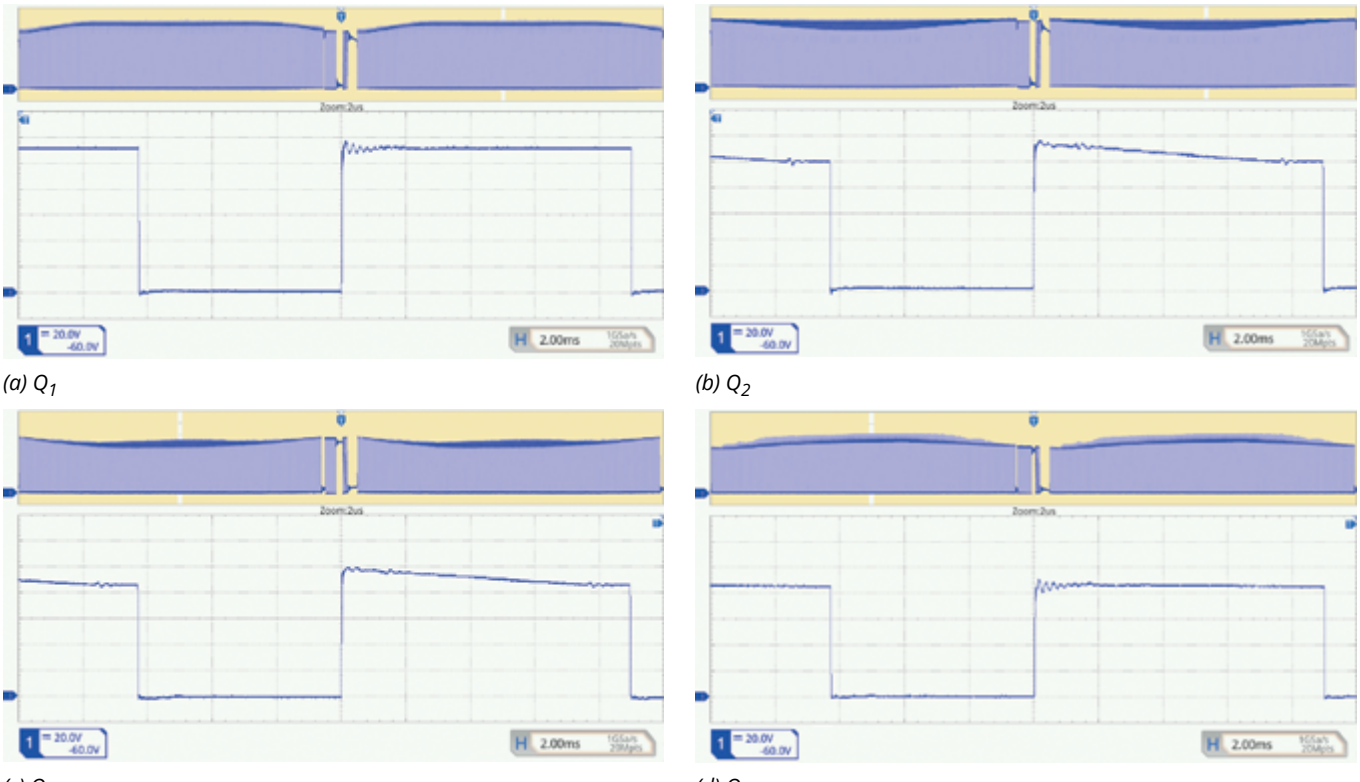
Figure 3 demonstrates the behaviour of V_{C1}, V_{C2}, V_{C3}, and V_{Cbulk} during different operating conditions. Evidently, the voltage balance is well maintained not only at steady state but also during transient responses. The worst-case scenario for the outer cell occurs during a differential-mode surge as demonstrated in Figure 3(c). The converter quickly increased V_{C3} in response to the fast variation in V_{Cbulk}, which maintains the operating voltage for the outer cell MOSFETs well within the 150V limit.

Mind The Loop

In addition to the operating voltage, the overshoot during MOSFET turn-off transitions needs to be controlled in order to meet the design requirement. Turn-off overshoots in general are a function of parasitic inductance and reverse recovery current. Most commercial 150V MOSFETs already have excellent reverse recovery characteristics intended for hard switching applications; hence, minimizing parasitic inductance through PCB layout optimisation is a necessary step. Using SMD components and low ESR ceramic capacitors for loop size reduction is recommended. Figure 4 exemplifies a PCB design in which 8 x SO8 MOSFETs and SMD flying capacitors are arranged to minimize 4 loops formed by (Q_4, Q_5, C_1), (Q_6, Q_3, C_1, Q_2), (Q_7, Q_2, C_2, C_3), and (Q_8, Q_1, C_3, C_{bulk}, R_{cs}). The two film-type PTH capacitors in parallel with C_2 are not included in Figure 4 for ease of demonstration.

Thanks to low loop inductance and excellent reverse recovery performance, the switching waveforms of MOSFETs Q_1, Q_2, Q_7, and Q_8 exhibit clean transitions with minimal overshoots. Even for the maximal loading condition as illustrated in Figure 5, the overshoot is less than 10V and all switching components in the outer cell experience less than 120V. This suggests an operating margin of 30V or 20% which is very desirable for hard-switching applications.

Similarly, the Drain-to-Source voltage of other 4 MOSFETs Q_3, Q_4, Q_5 and Q_6 also undergoes minimal overshoot and ringing, resulting in maximal voltage stress of less than 120V. Due to space limit, the experimental data for the inner cell is not included in this article but can be provided upon request.



(a) Q_1 *(b) Q_2*

(c) Q_7 *(d) Q_8*

Figure 5: Drain-to-Source voltage of switching devices in the outer cell. The testing condition is 115Vac and 1.5kW. Experimental data were collected by a floating oscilloscope and a 300MHz single-ended probe. The 20MHz bandwidth limit function is disabled.

Stay Cool Stay Reliable

In addition to electrical stress, high operating temperatures greatly affect the life span of switching components in general and in particular 150V MOSFETs. A reliable design should be able to limit component temperatures while delivering maximal power to the load. This target is not easy to achieve if the converter is inefficient and the heatsink size is constrained.

Multi-level totem-pole PFC is thermally more advantageous than 2-level solutions thanks to more efficient power conversion and greater loss distribution. In particular, the 3kW multi-level totem-pole PFC prototype as shown in Figure 6 can achieve > 99.2% efficiency at 230Vac for 30% to 50% load, and has a total loss of < 38W at 100% load. The overall losses present in the switching leg is in the order of 20W which is distributed evenly between 8 MOSFETs. Therefore, each MOSFET has to dissipate around 2.5W at full load, which can be achieved by bottom-side cooling working in conjunction with thermal vias and thermal interface material.

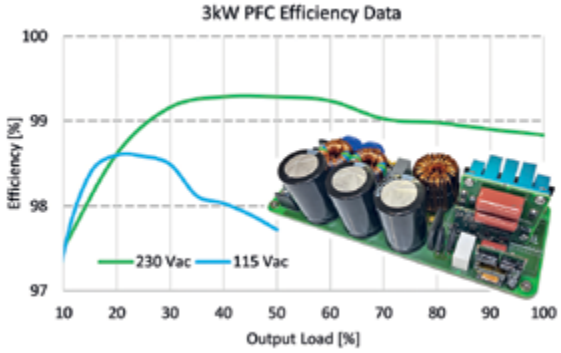


Figure 6: 3kW multilevel totem PFC prototype and efficiency data

Figure 7 shows a thermal image of 4 MOSFETs in the inner cell. The remaining outer cell MOSFETs are covered by the control card and cannot be seen in the image. The thermal data suggests that the maximal absolute temperatures of the 4 switches are well below 50 degrees Celsius at full load and minimal air flow. The temperature rise above the ambient temperature is 30 degrees Celsius. This ties in well with the efficiency data and the estimation of power loss per MOSFET. It is important to stress that having the power switches running cooler is the most effective way to improve the product reliability.

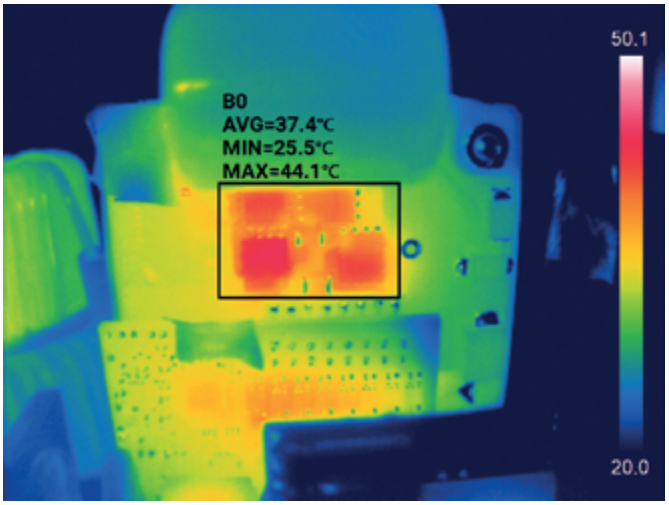


Figure 7: Temperatures of Q_3, Q_4, Q_5, and Q_6 captured at V_{line} = 230V and P_{load} = 3kW. Measurements were taken after 20 minutes running at the ambient temperature of 20 degrees Celsius. Air flow is < 0.3m3/min.

Summary

Using 150V MOSFETs for 400V power conversion does not make the design less reliable if all switching devices are controlled to operate well within their electrical and thermal ratings. As demonstrated in the article, multilevel bridgeless totem-pole PFC can be designed to operate well within their safe operating area with significant margins at extreme conditions and be as reliable as any other topologies. By controlling the flying capacitor voltages, the voltage stress for 8 x 150 MOSFETs remains within 120V at steady state and 150V for line voltage surges and transients.

Thermally, the multilevel totem-pole PFC offers advantages over 2-level solutions because multilevel power conversion is more efficient (>99.3% efficiency), leading to lower power losses and heat generated. Additionally, multiple switching components spread the losses over more switches, minimizing the risk of thermal hotspots commonly associated with a 2-level design.

References

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