Gate Drive Optimisation

1. Background

Driving of gates of MOSFET, IGBT and SiC/GaN switching devices is a fundamental requirement in power conversion. In the case of ground-referenced drives this is relatively straightforward and can use conventional silicon design. For floating gates, life gets more interesting, in that there is a twin challenge. Fast level shifting needs to be achieved, and getting the gate drive power to the driven device. In addition, demands for low quiescent power and for fast transitions in burst-mode operation impose additional requirements.

2. Towards the Ideal Gate Driver

The "wish list" for a gate driver product range will include:

- Robust, reliable operation under all operating conditions
- Low cost, particularly if significant numbers are to be used such as in multilevel deployments
- Zero quiescent power
- Minimal (ns scale) propagation delay and excellent time matching – particularly in half-bridge deployments and for driving series MOSFETs
- Complementary operation with interlock and adjustable deadtime
- Fully-floating operation with galvanic isolation
- No need for local powering – i.e. completely avoiding bootstrap and/or local power source requirements and start-up complications
- "Instant" response to drive signals, particularly when the device has been quiescent for some time
- Wide duty range with fast changes of duty cycle – as for example in totem-pole PFC deployment
- Low impedance unpowered pulldown of the gate of the driven FET
- Compatibility with GaN, SiC devices as well as Si MOSFETs and IGBTs
- Consistent technology approach for functional insulation, basic insulation and reinforced insulation requirements
- Standardised low-cost solution for all common switch drive requirements

ICERGi has focused on meeting these requirements with its "TruDrive™" approach.

3. Level Shifting and Gate Powering – two key tasks

Level shifting can be done "in semiconductor" with isolation wells and resistive or capacitive signal transmission, with challenges relating to trade-offs between propagation delay and power consumption, ability to handle voltage spikes including negative ringing on the switch node etc. Level shifting can also be undertaken using magnetic approaches, such as by modulation of a high-frequency carrier or by edge-transmission. Full galvanic isolation, extending to reinforced insulation usage as required, is associated with magnetic approaches. These can be particularly attractive in deployments where on-chip solutions are not feasible.

Typically switches need drive current of up to several amps at voltages from ~5V(GaN) to ~15V (IGBT). The simplest approach is to provide power via a bootstrap arrangement, which can be effective in a half-bridge arrangement where there is an active pulldown of the switch node. In other topologies such as high-side buck or indeed multilevel topologies, this approach to local powering gets impractical, as is the case also with high voltages. Here, design challenges can include severe "ringing" on switch nodes, and managing extreme duty cycle ranges or constant "on" operating conditions as may be required.

Meeting this requirement can mean usage of local power supplies to supply power to the driver section associated with each switch. The demands on such supplies can be quite severe, in terms of their ability to handle the severe dV/dt conditions on the switch node. This drives a requirement for minimal capacitance in these local power supplies.

The TruDrive™ approach eliminates the requirement for this local powering. ICERGi devices effect direct gate drive power transfer, without the need for a plethora of local power sources, thus reducing cost and avoiding common-mode complications associated with these power sources.

These drives work alongside controllers optimised for multilevel/multiphase operation, with again a requirement for low-cost operation, complete with excellent transient management, protection features and other aspects typically demanded of high-end PFC controllers. State machines on ARM Cortex™ M0 devices, initially the ST™ STM32F0 types, are programmed in low-level C.

4. The ICERGi® TruDrive™ Implementation

The ICERGi designs approach the ideal "wish list" in all key areas. Miniature magnetics ensure a compact design with full galvanic isolation and at low cost, with zero quiescent power.
TruDrive™ technologies can be implemented to work with either PWM signals as traditionally found in most power supply controllers or with pulse signals. The latter implementation is optimised for digital controllers, such as ICERGi PFC and LLC Controllers, allowing full and precise control of latency, deadtime, and gate voltage. Pulse-drive signals are generated directly by the digital controllers without the need for an edge detector. This greatly benefits both manufacturing costs and design reliability.

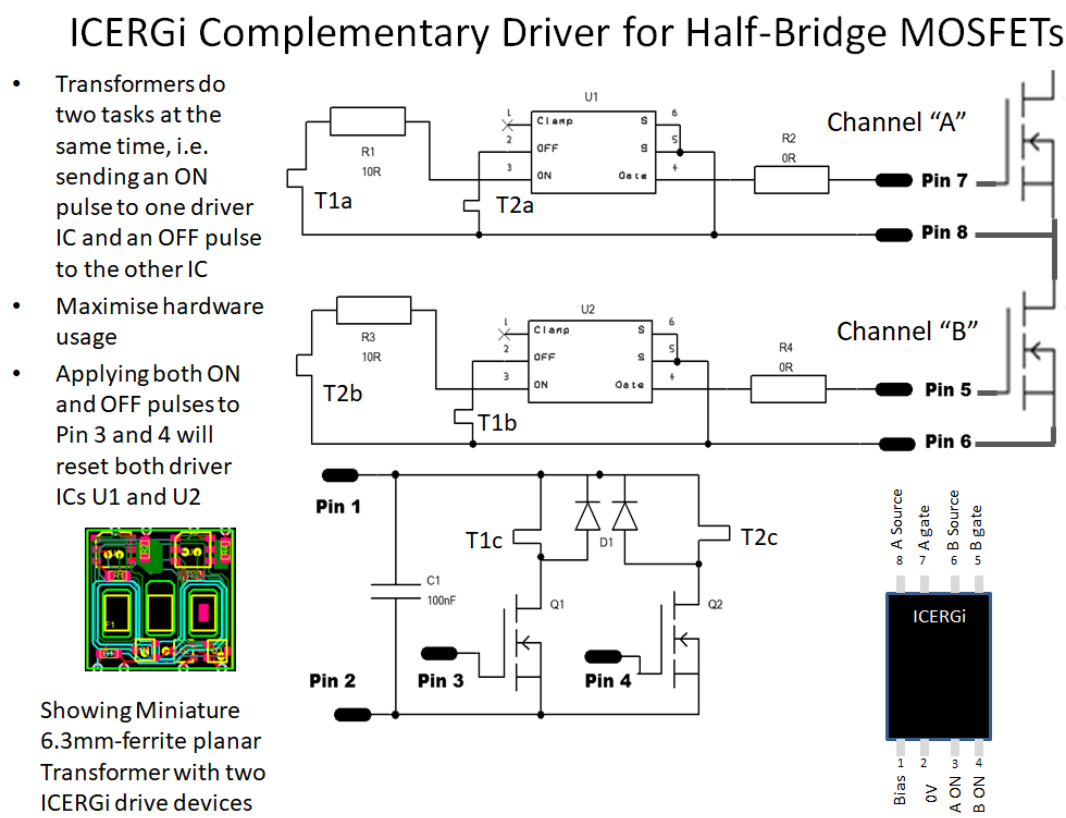

Fig. 1 Complementary Driver Basic Schematic, showing Pinout and Core Layout

Fig. 1 shows the outline schematic of a complementary gate drive approach, with magnetics implemented as planar (in-PCB) windings using both chambers of a miniature E6.3 ferrite core.

The ON pulse width reflects the maximum turn-on time budget for the device in question. This is typically 50ns for GaN types to ~150ns for Si/SiC MOSFETs or IGBT types. The OFF pulse can typically be 20ns-40ns.

Of particular advantage is that the complementary device is configured in an arrangement giving functionality analogous to that of an XOR gate – and hence the term "XORCELL™ Technology". This means that a pulse applied to both inputs simultaneously turns off both drives, thus allowing simple interface to controllers, easy deadtime provision and preserving the key interlock functionality.

There is considerable merit in using two transformers – one for the "ON" pulse and one for the "OFF" pulse. This naturally aligns well with complementary operation in that the "ON" pulse for the upper device can form an "OFF" pulse for the lower device and vice versa.

This approach allows for simple low-voltage drive (compatible with semiconductor processes) and "natural" diode-type reset of each transformer, as duty cycle is low. These properties allow avoidance of series capacitance which can restrict duty cycle slew rates, and allow immediate "no-latency, no quiescent power" operation.

At the gate of the driven FET the key functionality implemented within the driver includes:

- OFF signal over-riding ON signal. At lower powers this can be affected using a shunting approach. The ON signal is fed via a resistor, and this allows clamping to the local 0V level. At higher powers a series-disconnect approach can be used – essentially the "ON" pulse is disconnected from the gate.
- Direct "ON" pulse transmission. There is a direct path, via the resistor and/or switch cited above, from the drive transformer to the gate of the driven FET.
- Low-impedance quiescent gate pulldown. This is affected using a low-threshold PMOS device, which can hold the driven gate typically within 300mV of the local 0V level.
- Safe default operation. In the absence of drive signals the driver will revert to its quiescent condition within ~70µs. This corresponds to a requirement for drive refresh with nominal periodicity of 20µs to 30µs, thus requiring no refresh for operating frequencies above 60KHz.
- Fast turn-off. The PMOS device can be adequate at lower power levels but usage of a supplemental NMOS device can provide greater current rating and achieve pull-down of the driven gate closer to the local 0V level.

Key advantages may then be summarised.

5. Key Advantages

A benchmarking of the ICERGi approach is evident from consideration of Fig. 2.

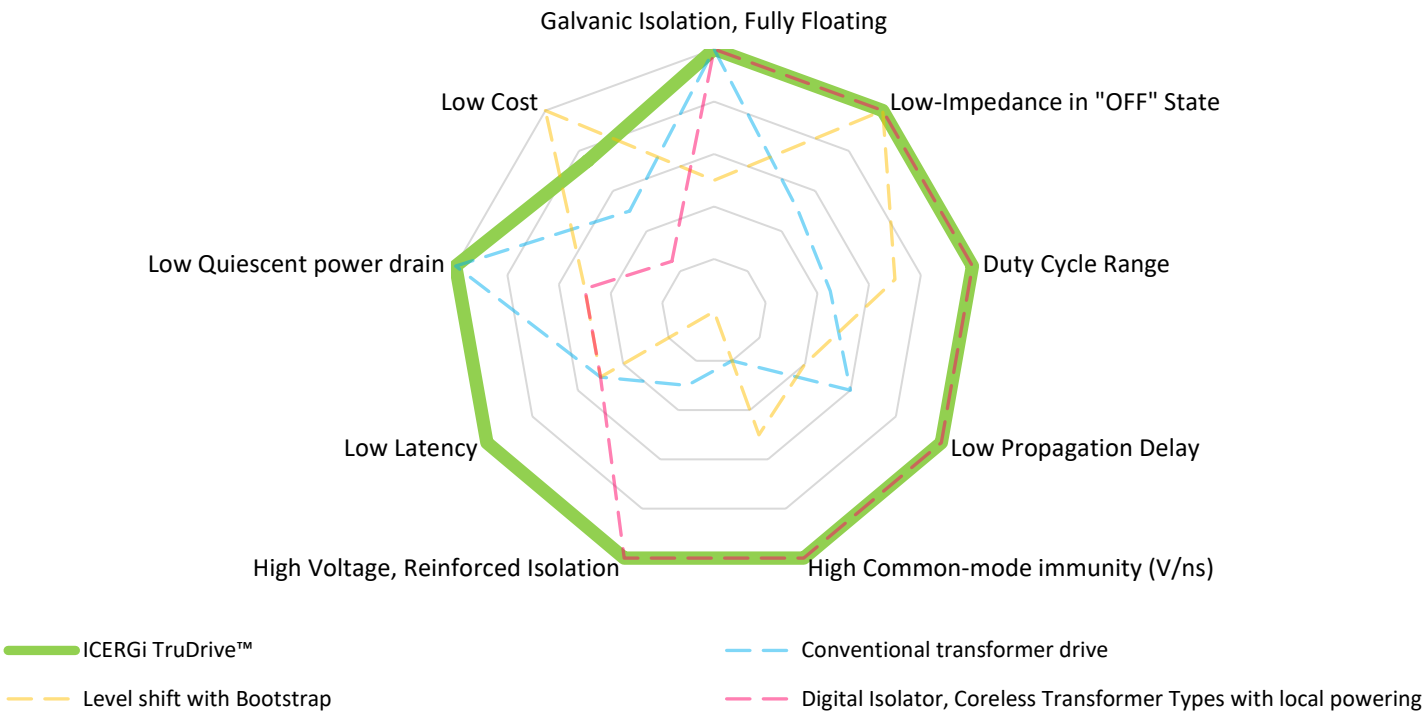

Fig. 2 Benchmarking of ICERGi TruDrive™ approaches vs alternatives

The close matching that can be achieved is also suited to implementing parallel or series operation of power MOSFET devices. Typically, lower-voltage types will have superior characteristics to devices with higher voltage ratings and thus a "composite device" using series-connected MOSFETs with TruDrive™ solutions can be attractive.

ICERGi drivers are compact and can be typically deployed in 9mm x 9mm for functional isolation (~600V) or 13mm x 9mm for basic insulation (~2kV).

Versions are available for MOSFET, IGBT, SiC, GaN devices.

6. Typical Deployment Applications

Typical deployments of ICERGi drivers in various topologies are shown below:

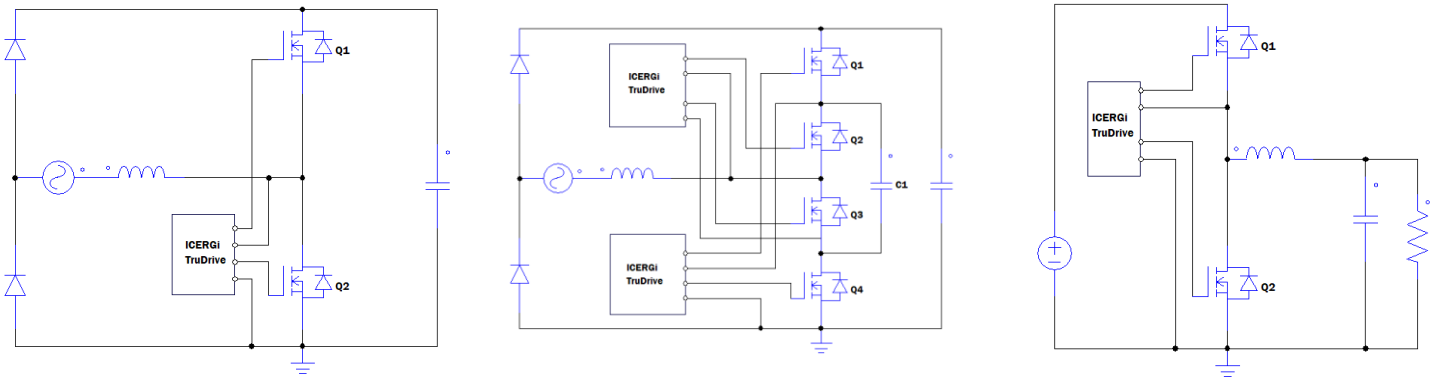

Fig. 3 Deployment of drivers in (a) (left) 2-level totem-pole PFC, (b) (centre) multilevel totem-pole PFC and (c) (right) synchronous buck

A 2-level (conventional) totem pole as in Fig. 3(a) is suited to usage of SiC or GaN devices with the attractive characteristics of the ICERGi TruDrive™ implementation being of value. This is even more apparent in multilevel Totem Pole implementations – feasible with lower voltage stacked silicon – with an outline schematic as in Fig. 3(b). The absence of local powering needs is of particular value in this deployment. The synchronous buck stage as shown in Fig. 3(c) benefits from precise timing and also by reduced control complexity as the high-side device can be turned on initially, and the lower device can operate in diode mode as desired by suppressing drive pulses using the "XORCell™" functionality.

Active clamp forward and flyback converters typically require operation of the clamp FET at voltages that may go too close to ratings of available IC devices, with the ICERGi range capable of giving the needed isolation and complementary operation with controlled deadtimes. Fig. 4 also shows usage in "cross-barrier" drive of synchronous rectifiers and in motor-drive deployments.

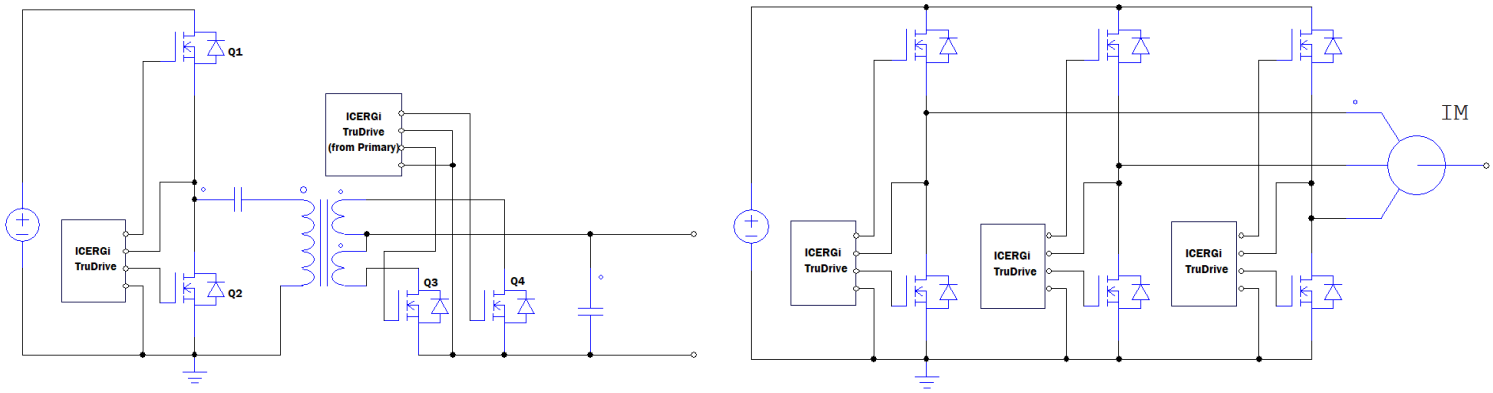

Fig. 4 Additional Deployments of ICERGi TruDrive Technologies – showing isolated synchronous rectifier drive (a)(left) and Motor Drive usage (b) (right)

7. Product Implementations

ICERGi has implemented the TruDrive™ technology in a wide range of "captive" in-house deployments, primarily for high-efficiency multilevel converters up to 3kW rated power at industry-leading efficiencies. This includes primary-derived drive of synchronous rectifiers across a reinforced-insulation isolation barrier. The ICERGi product numbering scheme for drivers is as in Fig. 5.

ICERGi Gate Driver Selection Guide: IC92 - X X X

	Input Type	Output Type
IC92 - **X** n n		
0	Pulse	Dual
1		Single
2	PWM	Dual
3		Single

	Rated Voltage	Class
IC92 - n **X** n		
0	600V	I
1		II
2		III
3	2kV	I
4		II
5		III
6	5kV	I
7		II
8		III

	Dead Time Type	Level Count
IC92 - n n **X**		
0	**Software**	2
1		3
2		5
3		ISO
4		-
5	**Hardware**	2
6		3
7		5
8		ISO
9		-

All Other

IC92 - 0 n n ONLY

CLASS I	$V_G \leq 5V$ $F_{SW} \leq 2MHz$
CLASS II	$V_G \leq 10V$ $F_{SW} \leq 500kHz$
CLASS III	$V_G \leq 17V$ $F_{SW} \leq 200kHz$

Fig. 5 ICERGi Gate Driver Selection Guide

ICERGi also makes available products for independent usage, and offers a custom design capability in this area. Examples of ICERGi implementations, including drive arrays for multilevel conversion, are as in Fig. 6.

Fig. 6 Examples of gate driver implementations – see also http://www.icergi.com/gate-drivers

These driver approaches are instrumental in ICERGi achieving best-in-class performance in AC-DC and DC-AC conversion, including at 99% peak efficiency.

8. Summary

Demanding operating conditions require innovation in gate driver technology, as brought with the ICERGi TruDrive™ technologies. This technology set allows for a standardised low-cost and high-performance approach delivering simplified designs in very compact footprints. Typical applications include driving MOSFET, IGBT, GaN, and SiC switches in multiple applications such as Inverters, AC-DC/DC-DC Switch Mode Power Supplies, Class D amplifiers and Motor Drives.