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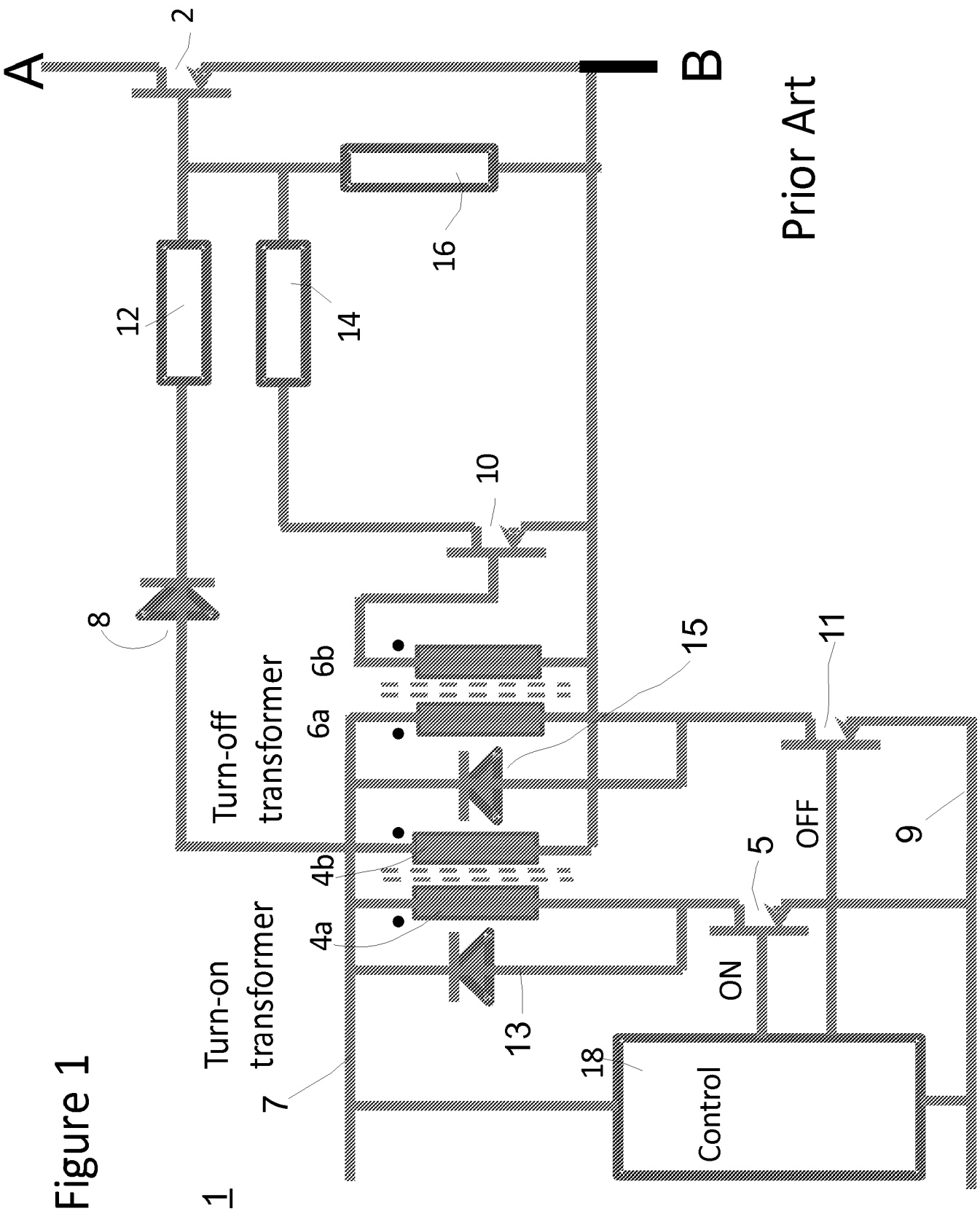

A
B
Prior Art
2
16
12
14
10
8
15
11
6b
6a
Turn-off
transformer
4b
4a
Turn-on
transformer
5
OFF
9
ON
13
18
Control
7
1

Figure 1

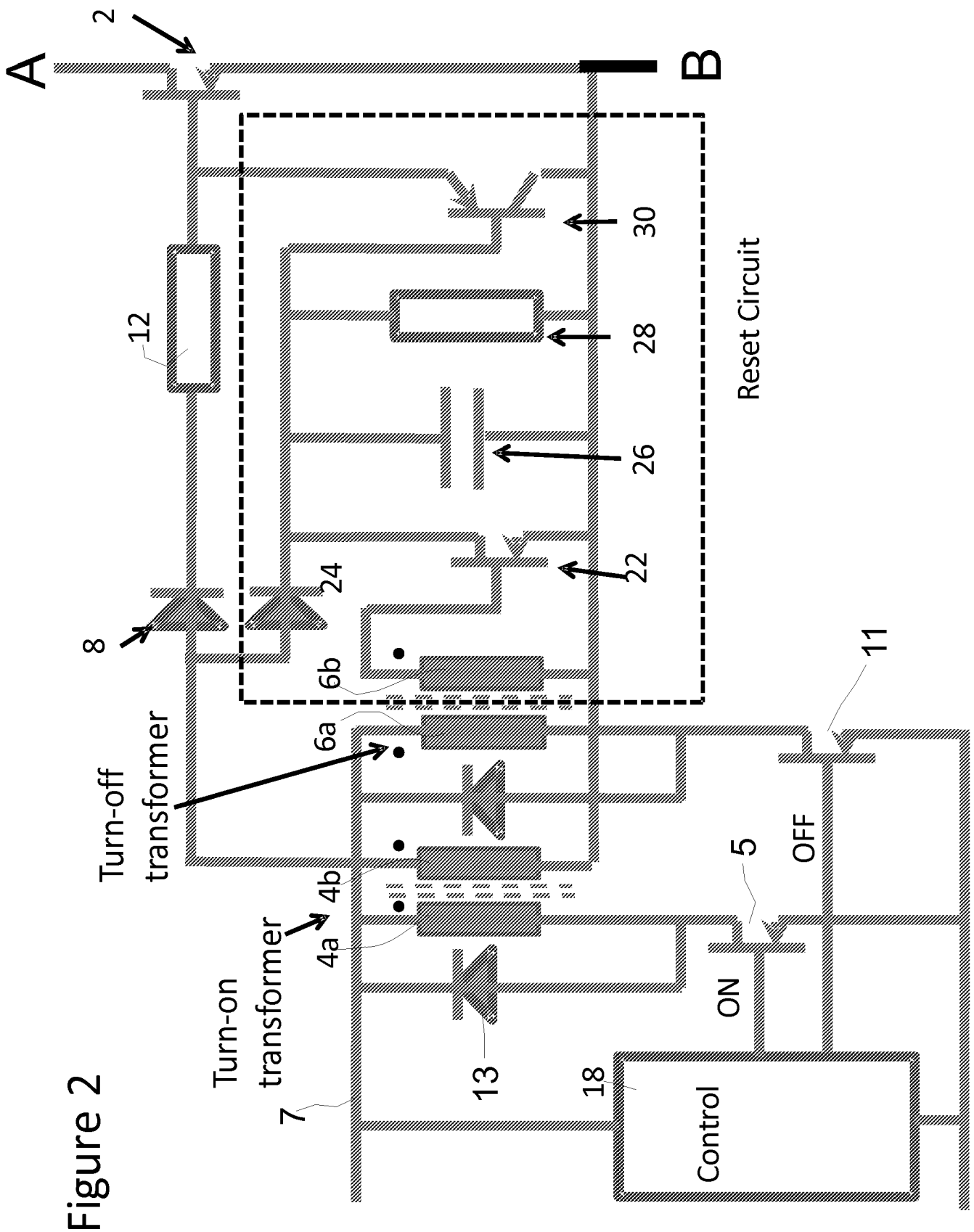

A
B
2
30
28
26
22
24
12
8
6b
6a
4b
4a
13
7
18
Control
ON
OFF
5
11
Turn-off transformer
Turn-on transformer
Reset Circuit

Figure 2

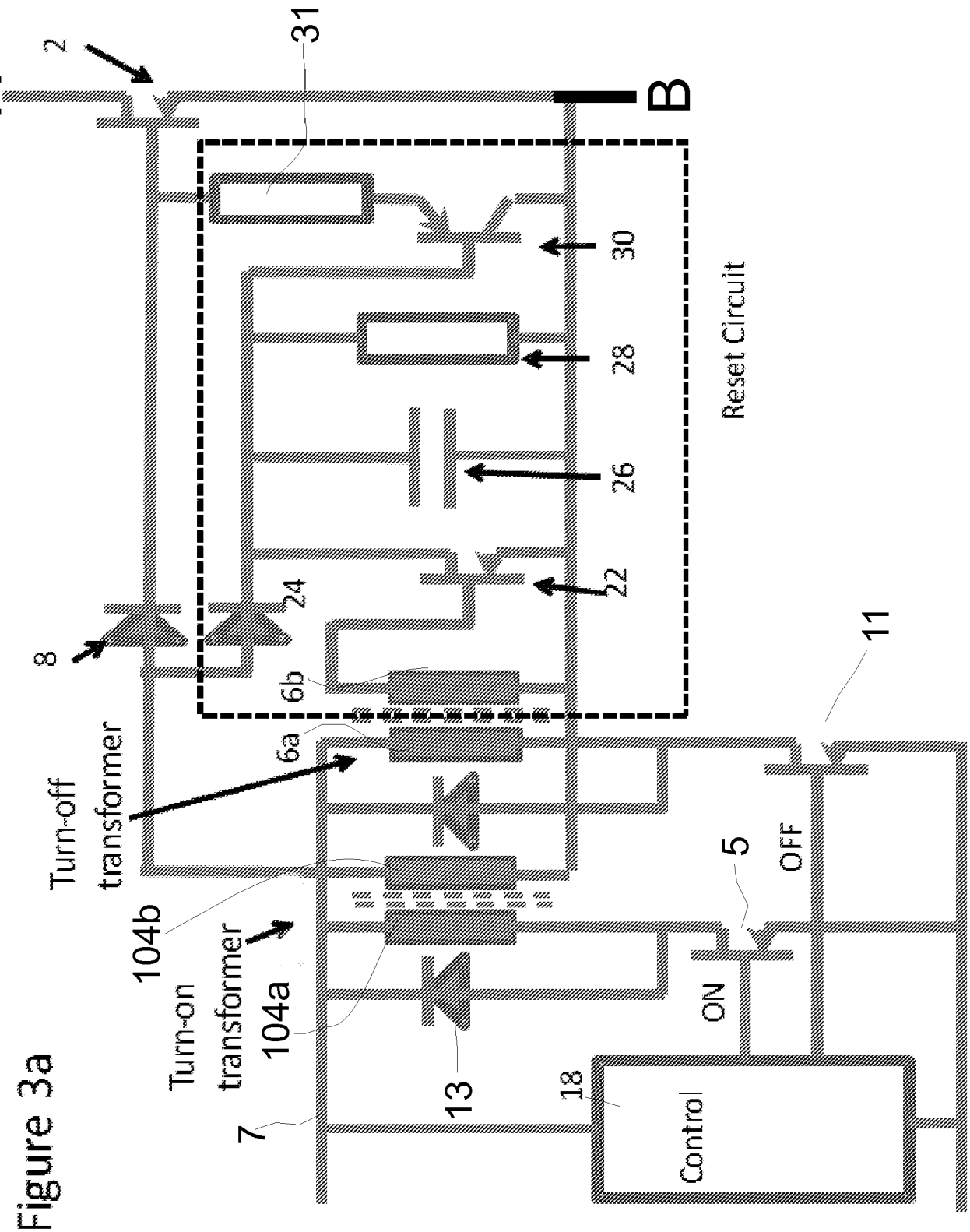
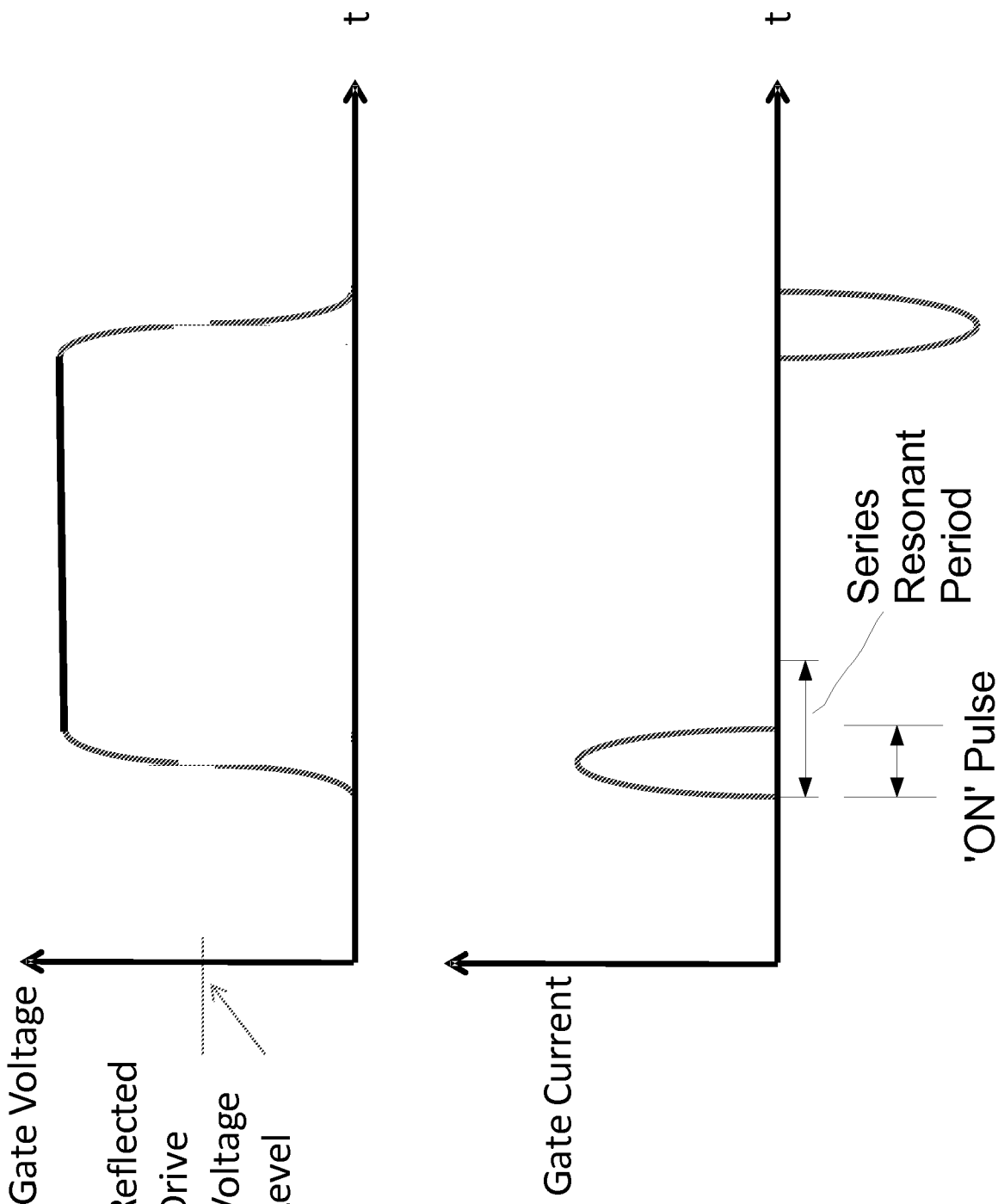

A
B
2
31
30
28
26
22
24
Reset Circuit
8
6b
6a
Turn-off transformer
104b
Turn-on transformer
104a
7
13
18
Control
ON
5
OFF
11

Figure 3a

Figure 3b


Gate Voltage
Reflected
Drive
Voltage
Level
t
Gate Current
t
Series
Resonant
Period
'ON' Pulse

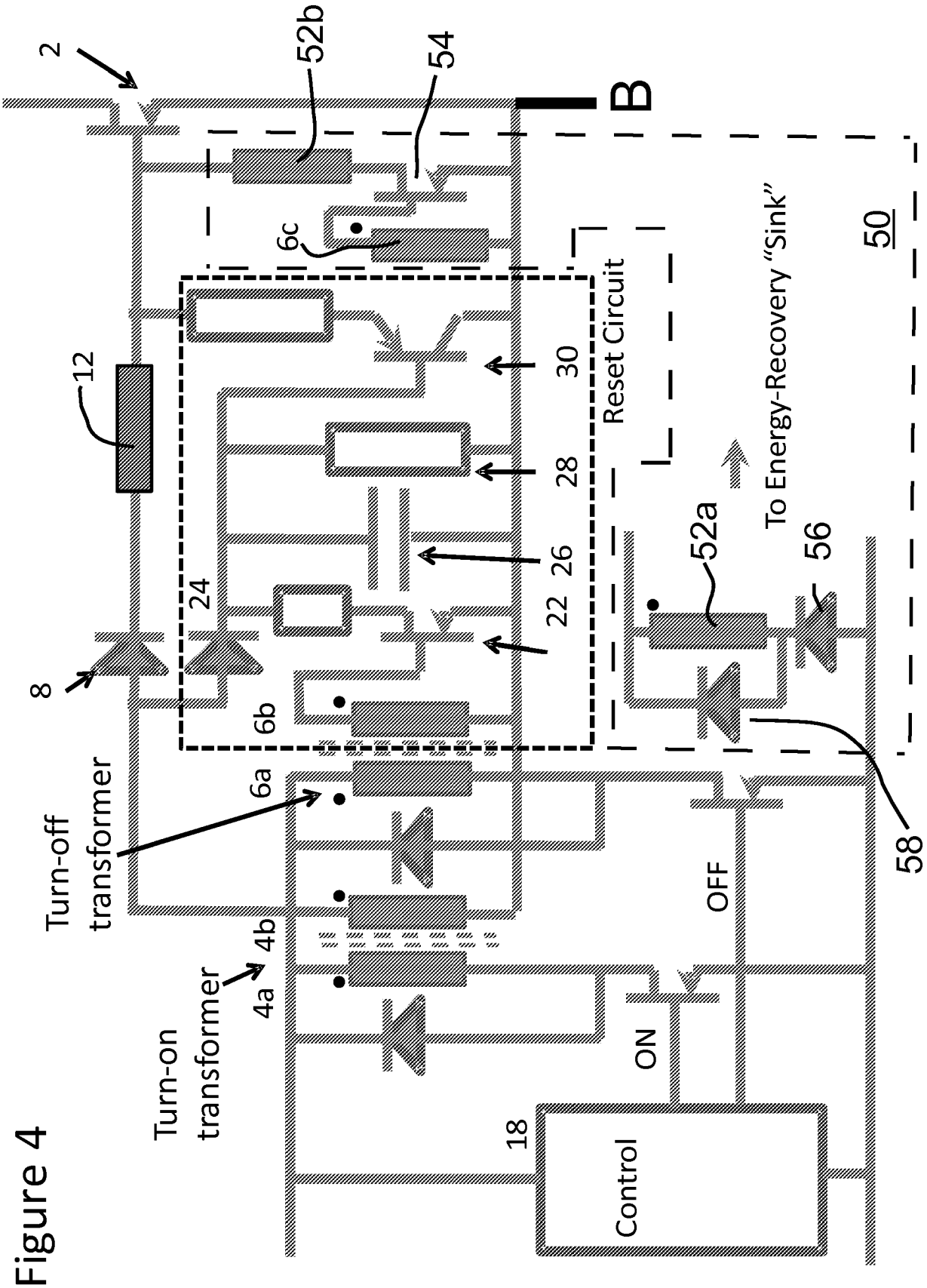

A
B
2
52b
54
6c
12
30
28
26
22
24
8
6b
6a
Turn-off transformer
4b
4a
Turn-on transformer
18
Control
ON
OFF
Reset Circuit
50
52a
56
58
To Energy-Recovery "Sink"

Figure 4

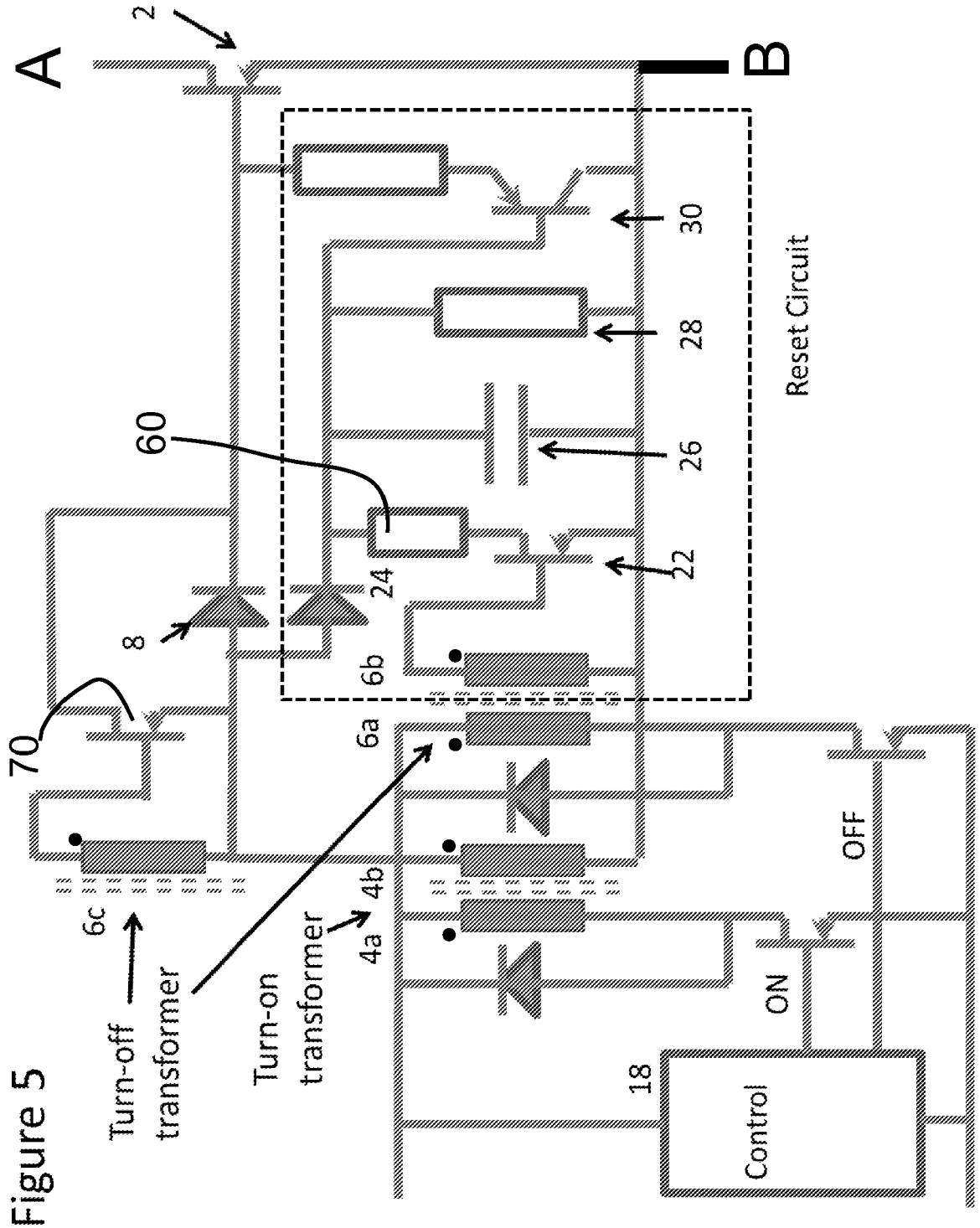

A
B
2
30
28
26
22
24
60
8
70
6b
6a
6c
4b
4a
Reset Circuit
Turn-off transformer
Turn-on transformer
OFF
ON
18
Control

Figure 5

A GATE DRIVE CIRCUIT FOR A SEMICONDUCTOR SWITCH

Field of the Application

The present application is directed to drive arrangement for semiconductor switches and in particular to a method of driving the gate of a switch with pulses corresponding to turn-on and turn-off commands.

Background

The present application is directed to isolated gate drive circuits which are employed to control the operation of semiconductor switches. Isolation is frequently desirable when controlling semiconductor switches. Examples of situations where isolation is desirable include when voltages being switched by a semiconductor switch are relatively high compared to those employed in the control circuit controlling the operation of the semiconductor switch or when a "floating" semiconductor switch is used or if drive is to be effected across an isolation boundary.

A common approach to driving the gate of a semiconductor switch, such as a MOSFET, employs a drive transformer in which a drive signal is generated and applied to the primary side winding of the drive transformer. The output from a secondary winding of the drive transformer is used to provide a turn-on voltage to the gate of the semiconductor switch. In this configuration, the width of the drive signal T_{drive} substantially determines the ON time T_{ON} of the semiconductor switch, i.e. the semiconductor switched is caused to be turned on at the start of T_{drive} and once the T_{drive} finishes the semiconductor switch starts to turns off. A disadvantage of this approach is that a relatively large transformer is required.

A less common approach and one which is employed generally in the present application is to employ a drive circuit in which a first pulse is provided to turn on the semiconductor switch through a first transformer (turn-on transformer). In contrast to the previous approach, the duration of the pulse does not dictate the ON time of the semiconductor switch. A separate pulse is employed through a second transformer (turn-off transformer) to cause a reset circuit to turn off the semiconductor switch. As a result, the ON time of the semiconductor switch is dictated by the delay between the first and second pulses. An exemplary arrangement for such an isolated gate drive circuit is shown in Figure 1 for the operation of a switch 2 for switchably connecting a first node (A) to a second node (B). In this circuit 1, a first control pulse, hereinafter referred to as an 'ON' pulse, is generated by a control circuit 18 and applied to the primary windings 4a of a first pulse transformer 4 in the exemplary circuit by means of a switch 5 connecting the primary between a supply voltage 7 of the control circuit (frequently referred to as a bias rail) and a control circuit ground 9 in response to a control signal from the control circuit 18.

Typically the 'ON' pulse may have a duration of 50ns to 100ns. The output from the secondary winding 4b of the first pulse transformer is provided across the gate and source of the semiconductor switch 2, which may for example be a MOSFET, IGBT or similar voltage driven semiconductor switch. For the purposes of explanation, the operation of the circuit will now be described in the context of where the semiconductor switch is a MOSFET 2. One side of the secondary winding 4b is connected directly to the source of the MOSFET. The other side of the secondary winding 4b is connected through a rectifier 8 to the gate of the MOSFET. When an ON pulse is applied to the primary winding 4a of the first pulse transformer, a corresponding pulse is presented on the secondary winding which is directed to the gate of the MOSFET through the rectifier 8 turning the MOSFET on. Because of the presence of the rectifier 8 the gate capacitance holds the pulse voltage thus maintaining the MOSFET in an ON state once the ON pulse has finished. As a result, the duration of T_{on} is not dictated by the length of the ON pulse, thus allowing for a shorter duration pulse to be employed. A resistor 12 is provided in series with the rectifier 8 to limit the current. The resistance value of the resistor may be selected to slow the rise time of voltage on the gate of the MOSFET2 for EMI purposes. A rectifier (reset diode) 13 may be provided across the windings of the transformer to provide a path when the ON pulse finishes and the first switch turns off.

As the rectifier 8 effectively stops the MOSFET resetting when the ON pulse is removed, a separate reset circuit is provided to turn off the MOSFET. The reset circuit generally comprises a second pulse transformer 6. A primary winding 6a of this second pulse transformer is driven with a pulse, hereinafter referred to as an 'OFF' pulse from the control circuit 18, which in the case of the exemplary circuit is by means of a second switch 11 connecting the primary winding of the second transformer between a supply voltage 7 of the control circuit (frequently referred to as a bias rail) and a control circuit ground 9 in response to a control signal from the control circuit 18. A rectifier (reset diode) 15 may be provided across the windings of the transformer to provide a path when the OFF pulse finishes and the second switch 11 turns off. Usage of reset diodes 13, 15 limits voltage stress on switches 5 and 11.

The 'OFF' pulse has a similar duration to the 'ON' pulse. The secondary winding of the second pulse transformer provides a pulse to the gate of a second semiconductor switch10, which may be a small MOSFET. This second switch is connected across the gate and source of the first MOSFET 2. The 'OFF' pulse thus turns on the second switch10which provides a path for the gate capacitance of the first MOSFET to discharge thus turning off the first MOSFET 2. A resistor 14 may be provided in series with the second switch 10 to limit the speed of turn-off for EMI or other purposes. A disadvantage of this configuration is that there is a high impedance condition in either state between switching instants, which can render the device susceptible to conditions of spurious turn-on when the device has been commanded to be "off". This can be addressed in part by fitting a further resistor 16 across the gate and source of the MOSFET 2. However, whilst a low value of resistance is desirable

for noise immunity using a low value of resistance for resistor 16 causes material losses when the gate of the MOSFET 2 is driven high.

One problem with the arrangement is that significant energy is required to cause the semiconductor switch to turn ON, with most of this energy wasted in the resistor 12. Eliminating the resistor does not solve the problem as the energy wastage is simply transferred to the rectifier 8 and problems of excessive current and EMI are introduced. Whilst these losses may be acceptable in low frequency switching circuits, the losses increase directly with frequency and as a result, the use of pulse transformer circuits in this manner is less desirable at higher frequencies because of poor efficiency and the requirement to dissipate heat generated in the drive and reset circuits.

A further problem is that losses in driving the gate of the semiconductor switch 2increase with frequency resulting in significant heat and power losses making the use of this configuration less desirable at higher switching frequencies.

Summary

A problem identified by the Applicant is that employing a circuit requiring two pulses with one to turn on a switch and a second to turn off a switch, a dangerous situation can arise if for some reason no 'OFF' pulse is received. The present application provides solutions to this identified problem, the problems identified above and others.

More particularly, the present application provides a 'fail safe' mechanism for an isolated gate drive circuit controlling a semiconductor switch for ensuring the semiconductor switch being controlled is turned 'off' in the event that no reset pulse is received. The 'fail safe' mechanism is triggered by the arrival of an 'ON' pulse turning on the semiconductor switch and automatically turns 'OFF' the semiconductor switch in the event that no 'OFF' pulse is received.

Thus an isolated gate drive circuit for controlling the operation of a first semiconductor switch is provided in accordance with appended claim 1.

The present application also provides for the use of LC resonance to cause the semiconductor to switch.

Using this approach, the requirement for a series resistor after the diode is eliminated, a lower turns ratio can be used and a smaller transformer may be employed, thereby significantly reducing losses.

The present application further provides an energy recovery circuit which recovers energy from the gate capacitance when a pulse is received to turn off the semiconductor switch.

Description Of Drawings

The application will now be described with reference to the accompanying drawings in which:

Figure 1 represents a known circuit using a pulse transformer to turn on a voltage driven semiconductor switch;

Figure 2 shows an embodiment of the present invention, wherein an isolated gate drive circuit for a semiconductor switch is incorporating a fail safe reset feature;

Figure 3a shows a further embodiment of the present invention, wherein an isolated gate drive circuit for a semiconductor switch using resonance in the gate drive circuit to assist turning on the semiconductor switch is shown;

Figure 3b illustrates exemplary waveforms of the present invention from the circuit of Figure 3a;

Figure 4 illustrates a further embodiment of the present invention wherein an isolated gate drive circuit with an energy recovery circuit for recovering energy from the gate is shown; and

Figure 5 illustrates another embodiment of the present invention, showing an isolated gate drive circuit with an alternative energy recovery circuit.

Detailed Description Of Drawings

A first arrangement provides a new isolated gate drive circuit as shown in figure 2 for switching a semiconductor switch 2. The isolated gate drive circuit has a number of common features with the circuit of Figure 1 and accordingly reference numerals employed are shared with Figure 1 where appropriate.
The drive circuit of Figure 2 for turning "ON" the semiconductor switch may be as described previously with respect to Figure 1. More particularly, a control circuit 18 is configured to provide a pulse to turn 'ON' a first switch 5 which in turn connects the primary winding 4a of a first transformer 4 between a supply voltage (V_{bias}) and ground (0V) causes the primary winding of the first transformer to energise.

The output from the secondary winding 4b of the first transformer is provided through a rectifier 8 and optionally series resistor 12 to the gate of the MOSFET 2. Thus the application of an 'ON' pulse to the primary winding is transferred across the isolation barrier of the transformer and effects a turning on the MOSFET 2.

The arrangement of Figure 2 employs a novel reset circuit for resetting MOSFET 2. In particular, a reset circuit is provided which is configured to turn off the MOSFET 2 within a predefined interval after the arrival of the "ON" pulse. This provides a fail safe mechanism which ensures the reset circuit operates. The predefined interval is suitably less than the interval between "ON" pulses (i.e. the switching period). The reset circuit may employ a timer triggered to begin upon the arrival of the "ON" pulse and expire after a predefined

interval. The reset circuit is suitably configured to turn off the MOSFET 2 when the timer expires. This will now be explained in greater detail with reference to an exemplary circuit in which a monostable is employed to effect the timer. The monostable has a stable state in which the gate voltage of the MOSFET is clamped and a metastable state in which the gate voltage of the MOSFET is not clamped. The monostable is triggered into the metastable state by the arrival of an "ON" pulse and resets to the stable state after a predefined time interval. The monostable may also reset in response to the arrival of an "OFF" pulse.

Thus with reference to the exemplary implementation of Figure 2, the monostable comprises a normally closed switch 30connected across the gate and source of the MOSFET so as to clamp the gate voltage of the MOSFET. The normally closed switch 30 may be a PNP transistor. The transistor is configured to generally clamp the gate and source of the MOSFET together at a relatively low voltage, i.e. below which the MOSFET can turn on. To allow the MOSFET to be turned on by an arriving 'ON' pulse, the normally closed switch 30is opened. This may be implemented, as shown, by providing an output from the secondary winding through a second rectifier 24 to operate the clamping transistor when an 'ON' pulse arrives. Thus the 'ON' pulse causes the clamping transistor to switch off. As the clamping transistor is switched off, the MOSFET may be turned on by the arriving 'ON' pulse.

In the exemplary arrangement shown the reset circuit comprises a parallel Resistor 28 – Capacitor 26 combination. The RC combination ensures that the clamping transistor turns back on (reset of monostable) within a predefined time, which as will be appreciated by those skilled in the art is defined by the RC time constant. Thus the reset circuit always resets within a predefined time, irrespective of whether or not a reset 'OFF' pulse is received. This ensures fail safe operation of the reset circuit to ensure turn off of the MOSFET. It will be appreciated that the reset circuit thus operates as a monostable having a stable state in which the switch 30 is closed causing the gate voltage of the MOSFET 2 to be clamped and a metastable state in which the switch 30 is open allowing the MOSFET to be turned on.

This fail safe reset circuit may operate in parallel to a conventional reset circuit for example as previously described with respect to Figure 1 which is responsive to the arrival of an 'OFF' pulse. In a configuration, as shown, in Figure 2, the fail safe functionality may be integrated with a reset circuit responsive to the arrival of an 'OFF' pulse. Such an arrangement is provided in Figure 2, in which a second transformer 6 is employed to transfer a second pulse ("OFF" pulse) from the primary side to the secondary side. The secondary winding of the second transformer is connected to a further semiconductor switch 22 which is positioned in parallel with the capacitor. An arriving 'OFF' pulse switches on the semiconductor switch 22 providing a low resistance path for the capacitor 22 to discharge. This in turn causes the clamping transistor to turn on (reset of monostable) thus turning off the MOSFET. It will be appreciated that the second transformer is not required to transfer power in the same manner as the first transformer which needs to charge the gate

capacitor, accordingly the second transformer may be any suitable isolated signal transfer device and is not limited to being a transformer. Thus for example, the second transformer may be replaced by an optocoupler.

The value of capacitor 26 is selected such that the time constant of the resistor 28 capacitor 26 combination is a small multiple, for example less than3 times the typical switching period, but not such as to clamp materially the voltage on the gate of MOSFET 2 prior to termination of the normal ON-state time of this device.

This prevents the clamp transistor from pulling the gate of the MOSFET low as soon as the gate drive turn-on pulse is removed. The usage of resistor 28 and capacitor 26 at the same time ensures fail-safe operation, if no pulse is applied for some time, to turn the MOSFET off.

Thus the exemplary arrangement of Figure 2 provides a fail safe reset mechanism. This mechanism is also employed in the exemplary arrangements of Figures 3, 4 and 5.

Figure 3 superficially appears to provide the same isolated gate drive circuit as Figure 2 with the series resistor 12 removed. However this is not the case as the circuit of Figure 3 requires a primary side "ON" pulse with a lower voltage than that of Figure 2 and uses less energy than that of Figure 2. This will now be explained.

In particular, in the arrangement of Figure 3, there is a path on the secondary side comprising the secondary winding 104b of the transformer, a rectifier 8 and the gate capacitance of the semiconductor switch 2.

The inductance in the secondary side path driving the gate of the switch 2 is chosen so that the inductance in combination with the gate capacitance of the switch has a resonant period (inverse of resonant frequency) which is in the region of the duration of the "ON" pulse, or more specifically

That T_{on} is approximately $\pi\sqrt{LC}$ where *L* is the inductance of the secondary path and *C* is the gate capacitance value of the switch.

The capacitance of the gate is dictated by the particular switch selected, which in turn is generally dictated by the switching requirements for the circuit in which the switchis employed the value of capacitance may generally be viewed as being predetermined or at least predetermined within a limited range. Accordingly, to ensure that a desired resonant period is provided, a circuit designer may design the secondary path inductance to match the switch selected to achieve a particular resonant period. It is to be observed that in a conventional circuit it is generally considered desirable to limit the inductance value in the secondary path to avoid ringing. In contrast, in the arrangement of Figure 3 an increase in the inductance value is generally required. In one variation, this may be achieved by designing the transformer 104 to have significant leakage inductance. It may also be

achieved by including a discrete inductor in series with the windings or indeed a combination of the two.

The effect of matching the inductor and capacitor to obtain a desired resonant frequency will now be discussed with reference to the timing waveforms of Figure 3b.

In particular, as an 'ON' pulse is applied to the primary and its voltage is reflected from the primary windings across to the secondary windings by the turns ratio, the secondary current starts to increase along with the gate voltage. Whereas normally, the gate voltage would stop at the level of the reflected 'ON' pulse or just below it taking into account the rectifier 8 drop at which point the rectifier 8 would turn off, in the arrangement of Figure 3, the resonant LC circuit causes the gate voltage to increase further, upto approximately twice the reflected 'ON' pulse voltage until the current drops to zero.

Thus the circuit of Figure 3, gives a resonant drive, charging the capacitance of the power MOSFET (assuming this is linear) to approximately twice the open-circuit voltage as would be present across the secondary winding. As a result, this approach allows also for a reduction in the turns count of the transformer 104. At the same time, since the current is limited by the LC resonance, there is no need for the resistor 12 present in Figure 1 and 2. The control circuit providing the 'ON' pulse may be configured to provide an 'ON' pulse with a pulse width that equates to approximately half the LC resonant period so as to reduce losses. In this respect, approximately may be taken to mean within 30%, i.e. between .35 and .65 times the LC resonant period. It will be appreciated that a lower turns ratio transformer or a lower primary side pulse voltage or a combination of the two is required to turn on the switch compared to prior art implementations. Additionally, the losses are significantly less, since there are lower resistive losses owing the potential elimination of resistor 12. In an ideal circuit, losses are reduced by 50% and thus even accounting for non-idealities the potential energy saving is significant.

It may readily be determined whether a circuit is employing the principle outlined above since if it is the voltage of the pulse generated on the primary side times the turns ratio of the transformer is generally less than the gate voltage required to completely turn on the semiconductor switch, subject to nonlinearities in the effective gate capacitance of switch 2.. It will be appreciated that the control circuit on the primary side may use a lower voltage 'ON' pulse

Whilst the arrangement of Figure 3 provides for significantly reduced power consumption over the prior art, energy is still lost when the gate capacitance is discharged by the reset circuit to turn off the switch 2.

Figure 4 provides for an energy recovery circuit which recovers some of this energy when turning off the switch. Figure 4 provides an isolated gate drive circuit which transfers an 'ON' pulse generated on the primary side of a transformer to a secondary side to turn on a

switch on the secondary side. As the energy recovery aspect presupposes the switch 2 has been turned on, it will be appreciated that any of the arrangements previously described for turning 'ON' the switch 2 using a pulse may be employed. Whilst the previously discussed "fail safe" reset circuit of Figure 2 is presented in Figure 4, it will be appreciated from the discussion which follows that other reset circuits may be employed. Figure 4 provides an energy recovery circuit 50. This circuit is responsive to the 'OFF' pulse previously described. In certain configurations, there may be two 'OFF' pulses, with a first triggering the energy recovery circuit and a second triggering the reset circuit with a time delay between them to maximise the energy recovered. The energy recovery circuit provides an energy recovery transformer having a winding 52b switchably connected by a switch 54 across the gate capacitor of the switch 2, i.e. switchably connected across the gate and source of the MOSFET 2.

The switch 54 is responsive to the 'OFF' pulse. Accordingly, when an 'OFF' pulse is received, the winding 52b is connected across the gate capacitor allowing the capacitor to discharge through the winding. A further winding 52a on the energy recovery transformer, which may for example be on the primary side comprising the control circuit 18, recovers a part of this energy. This energy may for example be directed to the primary side bias supply. A rectifier 56 is provided in series with the further winding 52a to ensure the correct operation of the energy recovery circuit. A reset rectifier 58 may be provided in parallel with the further winding. The switch 54 may be operated by any suitable isolated signal transfer device such as for example an optocoupler. In the exemplary arrangement shown, the switch is operated by an additional secondary winding provided on the turn-off transformer transferring the 'OFF' pulse to the reset circuit. In this respect, a delay may be included in the reset circuit to delay the operation of the reset circuit so that energy recovery is maximised. In the exemplary circuit shown, this delay is implemented by including a resistor 60 in the path of the reset switch 22 so as to slow the discharge of the capacitor 26 through switch 22. Although, as explained above, this may also be effected by using different 'OFF' pulses for the energy recovery circuits and reset circuits with a suitable delay between them.

Figure 5 illustrates a further arrangement which combines the functionality of the energy recovery transformer and Turn-On transformer for delivering the 'ON' pulse to the switch 2.In this arrangement, a switch 70 is provided in parallel with the rectifier 8 employed to connect the secondary winding of the turn-on transformer to the gate of the switch. The switch 70 is operated by the turn 'OFF' pulse through a suitable isolated signal transfer device, which in the exemplary circuit, is a secondary winding of a turn-off transformer, which is also used to activate the reset circuit through a further secondary winding of the turn off transformer. Thus, when an 'OFF' pulse is received the switch 70 connects the gate of the MOSFET 2 across the secondary winding of the turn-on transformer allowing for energy to flow back to the primary side, thus allowing for the recovery of energy from the gate. To improve the effectiveness of the energy recovery process, the secondary winding of

the Turn-On transformer may be a tapped winding. In this configuration, the switch 70 may be employed to connect the gate to the tap of the winding rather than the full winding so as to provide a higher voltage on the primary side to assist in energy recovery.

It will be appreciated that several modifications are possible, for example, switch 70 and rectifier 8 may be combined, such that the body diode of switch 70 is used as rectifier 8. Equally, it will be appreciated that whilst the term rectifier may generally be taken to refer to diodes, it also includes other rectifying devices which may for example be active switched devices rather than passive.

Moreover, it will be appreciate that an advantage of the embodiments described is that default to a state in which the switch being controlled is OFF and at the same time present a low impedance at the gate which prevents accidental turning on of the switch by noise or parasitic coupling.

The isolated gate drive circuits described herein may be employed to operate any voltage driven switch and accordingly whilst the description may refer to the switch being a MOSFET, the application is not so limited. For example, the switch may be a IGBT. The switch in turn may be employed in a variety of switching applications including switching power supplies and motor drives. Exemplary, switching power supplies include for example, switched power factor correction circuits, switched "LLC" resonant circuits, flyback converters and synchronous rectifiers.

It will be appreciated that whilst several different embodiments have been described herein, the features of each may be advantageously combined together in a variety of forms to achieve advantage and that variations are possible. Whilst the 'OFF' pulse and any associated reset mechanism has been described with reference to ensure that a single switch is turned off, the same arrangement may be used in situations where multiple switches are required to be switched off. This is particularly useful in situations where the two or more switches share a common ground, for example in situations where the switches are employed as synchronous rectifiers.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, the connections may be any type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless

implied or stated otherwise the connections may for example be direct connections or indirect connections.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention. It will be understood that whilst particular polarity devices, e.g. PMOS, NMOS, PNP or NPN may be illustrated in the figures, that alternative polarity devices may be employed by appropriate modification of the circuits.

It will be appreciated that the present application has been described generally in the context of isolated gate drives. It will be understood that this refers to the use of a transformer to provide a drive signal to a switch. The provision of a drive signal to a switch may not be for isolation as such but may for example be for level shifting to provide a higher voltage drive signal from a low voltage control circuit.

Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operation may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments. However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements

or steps than those listed in a claim. Furthermore, Furthermore, the terms “a” or “an,” as used herein, are defined as one or more than one. Also, the use of introductory phrases such as “at least one” and “one or more” in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as “first” and “second” are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. An isolated gate drive circuit controlling the operation of a first semiconductor switch, the isolated gate drive circuit comprising:
a first transformer for transferring a first ('ON') pulse from a primary side of the first transformer to a secondary side of the first transformer to provide a voltage through a first rectifier to the gate of the first semiconductor switch to cause the semiconductor switch to be turned on,
a reset circuit comprising a monostable circuit having a stable state and a metastable state, wherein the monostable circuit is configured to be triggered into the metastable state by the arrival of the first pulse, the monostable circuit comprising a second semiconductor switch configured to clamp the gate voltage of the first semiconductor switch when the monostable circuit is the stable state, wherein the monostable is configured to be reset in response to the arrival of a second ('OFF') pulse.

2. A circuit according to claim 1, wherein in the metastable state of the monostable the second semiconductor switch is configured to not clamp the gate voltage of the first semiconductor switch.

3. A circuit according to claim 1 or 2, wherein the monostable comprises a resistor-capacitor combination, a voltage in the resistor-capacitor combination effecting the operation of the second semiconductor switch.

4. A circuit according to any preceding claim, further comprising a second rectifier, wherein the first pulse is presented to the reset circuit through the second rectifier.

5. A circuit according to claim 4, wherein the second pulse is transferred from the primary side to the secondary side by means of an isolated signal transfer device.

6. A circuit according to claim 5, wherein the isolated signal transfer device is an optocoupler.

7. A circuit according to claim 5 wherein the isolated signal transfer device is a second transformer.

8. A circuit according to claim 1 or claim 2, wherein the monostable comprises a resistor-capacitor combination, a voltage in the resistor-capacitor combination

effecting the operation of the second semiconductor switch, the circuit further comprising:

a second rectifier, wherein the first pulse is presented to the reset circuit through the second rectifier, wherein the second pulse is transferred from the primary side to the secondary side by means of a second transformer and wherein a secondary winding of the second transformer provides a signal to a third switch to cause the discharge of the capacitor of the RC combination.

9. A circuit according to any preceding claim, wherein a secondary path is defined comprising the secondary winding of the first transformer, the first rectifier and the gate capacitance of the semiconductor switch and wherein the voltage of the pulse generated on the primary side times the turns ratio of the transformer is less than the gate voltage required to turn on the semiconductor switch and wherein the series inductance capacitance (LC) resonance of the secondary path is employed to cause the semiconductor switch to switch.

10. A circuit according to claim 9, wherein the inductance comprises the leakage inductance of the transformer.

11. A circuit according to claim 9 or claim 10, wherein the inductance comprises a discrete inductor provided in the secondary path.

12. A circuit according to any one of claims 9 to 11, wherein the series resonant period of the secondary path is approximately twice the width of the pulse.

13. A circuit according to claim 9, wherein the series resonant period of the secondary path is less than 5 times the width of the pulse.

14. A circuit according to any one of claims 9 to 13, wherein the series resonant period of the secondary path is greater than the width of the pulse.

15. A circuit according to any one of claims 9 to 14, wherein the series resonant period is within 30% of the width of the pulse.

16. A circuit according to any preceding claim, further comprising a control circuit for generating the pulse on the primary side of the transformer.

17. A circuit according to any preceding claim wherein the reset circuit comprises a switch for connecting the gate of the semiconductor switch to a transformer winding to recover energy from the gate.

18. A circuit according to claim 17, wherein the transformer winding is a primary winding on a second transformer.

19. A circuit according to claim 17, wherein the transformer winding is the secondary winding of the first transformer.

20. A circuit according to claim 19, wherein the secondary winding is tapped and where the transformer winding is the tapped winding of the secondary.