Flying Capacitor Voltage Imbalance Protection in Multilevel Bidirectional Inverters during Surge

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***Abstract* — Input voltage surge events due to lightning strike and short-term transients such as input voltage dips are of a significant interest when flying capacitor multilevel (FCML) inverters are considered. During these fast dynamic events charge balance of flying-capacitor(s) can be compromised. This paper presents a time-efficient and reliable surge detection method to prevent FC drift during input voltage transients in FCML single-phase PFC/inverter systems. The effect on flying capacitor(s) voltage is analyzed with the help of an operational bidirectional inverter simulation. The proposed technique is implemented and validated based on a highly efficient and modern 3-level bridgeless totem-pole (BTP) power factor correction (PFC) with bidirectional grid-tied capability.**

Keywords — surge detection, surge immunity, voltage dips, flying capacitor multilevel (FCML), bidirectional inverter, grid-tied, bridgeless totem-pole, power factor correction (PFC).

I. INTRODUCTION

For a number of years, the use of multilevel power conversion systems have become widespread in both academic and industry as one of the best choices for high power applications [1]. However, with a need for higher power handling and more sophisticated design of the overall system EMC immunity requirements should not be overlooked and taken more seriously during the design process. Conformity with standards such as IEC 61000-4-5 [2] of a market-ready bidirectional PFC/inverter often includes an appropriate inrush current handling as well as input voltage surge protection. It is not unusual to provide surge immunity up to 4kV (Class 4), particularly when the interconnections include outdoor cables along with a power cable. Very often, there may be a requirement to restore normal operation without destructive effects to the system after such high energy transients occur. At present, one of the main surge protection handling measures adopted by industry is to add varistors across the line terminals and/or high voltage clamping diodes in parallel with the circuit to be protected [3]. The absorption of surge current and clamping of the input voltage by these devices are essential. However, it may not be sufficient due to a significant disparity between input and output voltages leading to a certain amount of residual energy flowing to post-stage circuits. Consequently, compromised boost operation and output overvoltage can result in high frequency switching device(s) failure. Hence, it is desirable to stop all gate drive signals and inhibit switching operation as fast as possible. In the context of FCML power conversion systems, additional care must be taken to ensure that flying capacitor(s) charge balance is not compromised to dangerous levels.

Appropriate performance of a FCML PFC/inverter needs the balancing of all capacitor voltages based on the number of levels used in the topology [4]. Unbalanced voltage can occur due to several reasons such as device tolerances, digital control timing delay, layout parasitics, etc. There are few ways to control the flying capacitor PFC/inverter such as using a natural balancing method, active (closed loop) method or a combination of both [5]. The natural voltage balance property allows for re-alignment of the flying capacitor voltage(s) after some time during a steady-state operation without a need of additional control strategy [6]. However, in contrast to closed-loop method, it is relatively slow and much dependent on a load type. Therefore, the natural charge balance cannot be guaranteed under realistic transient or steady-state operating conditions. An active method [5] is often implemented as a subset of a modulation scheme in which a duty cycle is adjusted to increase or decrease the charge/discharge time of the flying capacitor(s) to enforce the balance. However, only small duty ratio adjustments are usually generated and thus is proven ineffective during sudden high voltage transients.

The following article will study the effectiveness of the proposed surge detection method to prevent FC voltage imbalance in a bidirectional 3-level DC/AC inverter operated in a grid-tied mode. Fig. 1 illustrates a typical configuration in which a bidirectional DC/AC inverter enables the use of DC distribution systems in buildings, including renewable energy sources, energy storage, and a mix of AC and DC loads.

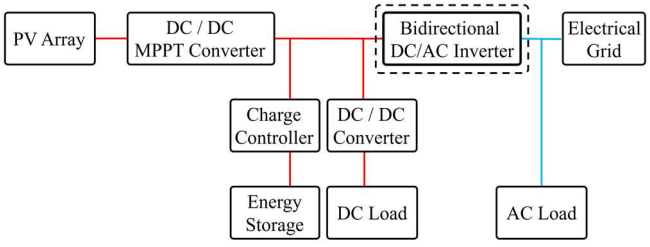

Fig. 1. Configuration of DC distribution systems integrated with a grid and a backup system.

II. Overview of Line Surge in 3-Level Bidirectional Bridgeless Totem-Pole PFC/Inverter

Consider a simplified schematic of 3-level bridgeless totem-pole PFC/inverter illustrated in Fig. 2 below. From the left side, the inverter arrangement consists of a synchronous rectification stage fitted with active devices Q_{SRL} and Q_{SRH} followed by a pair of inrush current diodes D_1 and D_2. The power stage is realized by main PFC inductor L_{main}, high frequency switching leg Q_{1-8}, additional flying capacitor C_{fly} for voltage division and output capacitor C_{bulk}. The string of MOSFET devices Q_{1-8} is controlled using a phase-shift modulation (PSM) in which switches Q_1, Q_2 and Q_7, Q_8 make up an outer phase and are driven in complementary fashion. The same applies to switches Q_3, Q_4 and Q_5, Q_6 forming an inner phase with an offset of 180°. The proposed modulation approach allows for the flying capacitor voltage to track the reference voltage of $V_{bulk}/2$. Provided that the natural charge balance condition of the flying capacitor is met, each pair of the series connected MOSFETs are subject to a potential difference of around 200V. This is also true for the converter nominal output voltage of 400V. The inverter is said to be operating with a nominal switching frequency of 65 kHz.

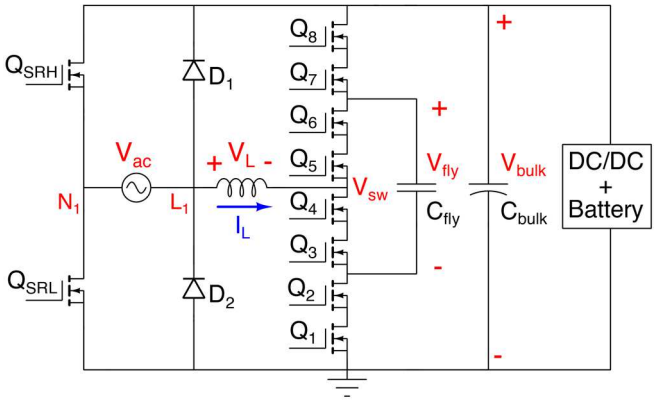

Fig. 2. High-level circuit diagram of a bidirectional bridgeless totem-pole (BTP) 3-level PFC/inverter.

To attain a good PF and comply with class B limits imposed by IEC 61000-3-2 [7], bidirectional PFC/inverter generally requires an adequate amount of filtering in order to provide a sufficient attenuation for both differential mode (DM) and common mode (CM) noise. An exemplary circuit consisting of a single CLC filter stage and a simple AC line protection circuit is provided in Fig. 3 below. Note that the actual implementation of the 3-level PFC/inverter requires an additional EMI filter stage. AC voltage is sensed using a differential amplifier with its inputs connected to both L_1 (Live) and N_1 (Neutral) terminals after a second stage of EMI filter.

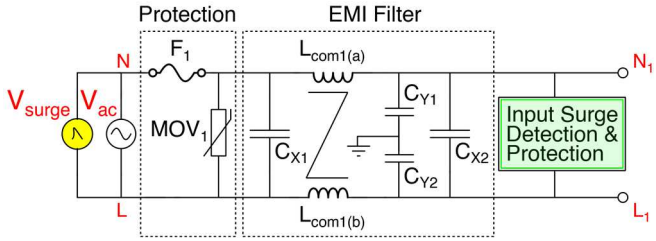

Fig. 3. Single stage CLC EMI filter with a line-to-line MOV_1 for surge protection and a single AC input line fuse F_1.

In the event of a recovery from short-term reduction in supply voltage or a differential surge, high voltage applied across the main inductor gives rise to excess current at any given switching period. This is particularly crucial during extreme cases i.e., positive 2kV differential surge pulse V_{sruge} at $\phi = 90°$ or $270°$ while the converter is operating with a minimum input voltage and a maximum output load. A conventional method to protect the sensitive circuitry involves detecting signs of excess current flowing in the inductor and/or abnormally high output capacitor voltage and subsequently triggering microcontroller to shut down the power stage. However, neither of these signals are present instantaneously and cannot be detected right away. In addition, the use of a digital controller and software-based protection against such events poses another concern regarding the latency from the time surge was detected until MOSFETs are fully switched off.

III. Proposed Surge Detection and Flying Capacitor Voltage Imbalance Protection Method

By using the above observations, a fast and effective method to input voltage surge detection is proposed (Fig. 4). In particular, upper and lower limits are imposed on the top of the input voltage V_{ac}.

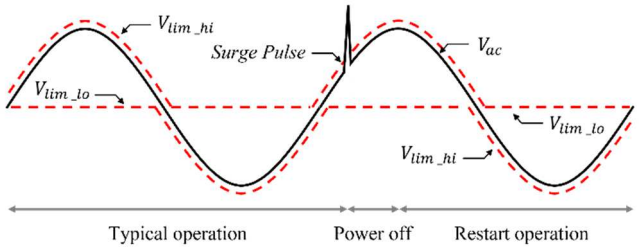

Fig. 4. Surge protection method based on out-of-bound voltage detection method.

Upper limit V_{lim_hi} during both positive and negative half line cycles provides a moderate band within which any disturbance of input voltage are considered to be benign and thus are neglected. This approach offers better robustness and precision as opposed to using a typical dV/dt detector. Both boundary signals are generated with the use of microcontroller. V_{lim_hi} is formed with the intention of reflecting the anticipated input voltage V_{ac} while V_{lim_lo} is more relaxed at a fixed voltage level. DAC data holding register is written by software and updated with a new input voltage tracking limit during each switching cycle. The new V_{lim_hi} value is calculated based on ADC sample of mains voltage V_{ac} signal.

For the sake of demonstration, this technique is achieved with a single differential amplifier and a low-cost ARM Cortex M0 microcontroller (Fig. 5). The advantage of such an approach is the superior responsiveness compared to a software-based surge detector method in a microcontroller. Besides, the structure is flexible and not limited to this specific arrangement of hardware.

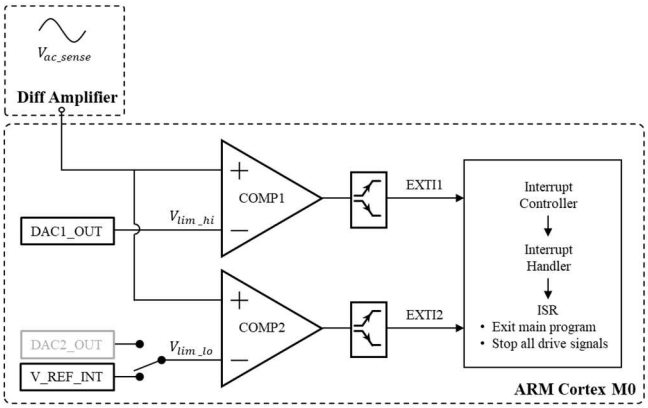

Fig. 5. Exemplary circuit to implement the proposed surge detection method based on a low-cost Arm Cortex M0 digital microcontroller.

For a digital implementation, input voltage V_{ac} is sensed by an auxiliary differential amplifier and fed into non-inverting inputs of both analogue comparators. During positive AC voltage digital-to-analogue converter (DAC1) converts and outputs software generated upper boundary V_{lim_hi} to an inverting input of COMP1. COMP2 inverting input is configured with a fixed voltage reference signal corresponding to V_{lim_lo}. The polarity of both comparators are configured to output low during a normal operation and high once either of the boundary limits are violated. Note, that during a negative AC input voltage, both comparator output polarities are inverted so that the same configuration can be used. Any low to high transition will immediately generate an interrupt on a dedicated EXTI line. It is then handled by an interrupt controller and in turn redirected to an appropriate ISR to shut-down all PWM signals to PFC switching devices. As soon as the transient event is over and all signal measurements are nominal, the controller enables all drive signals back and the operation is resumed.

It is recommended that the collar offset is chosen carefully with sufficient margin so that false triggering can be avoided in case of a significant grid voltage distortion, voltage sampling errors, etc. Furthermore, it is a good practice to limit boundary levels to some fixed value as the AC voltage approaches zero.

A. Alternative Voltage Boundry Generation Methods

Based on a microcontroller peripheral resource availability such as DACs and analogue comparators alternative surge detection boundary forming methods can be achieved.

1) Two Analogue Comparators with two DACs

With the addition of an external digital-to-analogue converter or a microcontroller with at least two DACs lower boundary signal V_{lim_lo} can be generated to track the input voltage with a fully adjustable band gap (Fig. 6).

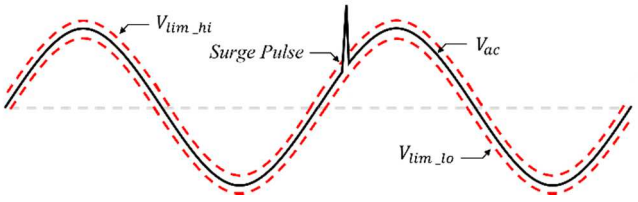

Fig. 6. Alternative voltage boundary forming method using a pair of two comparators and two digital-to-analogue converters.

One of the methods to derive a lower boundary can be realized by simply offsetting the upper limit by twice the allowed margin.

$$V_{\mathrm{lim}\_lo} = V_{\mathrm{lim}\_hi} - 2(V_{\mathrm{lim}\_hi} - V_{\mathrm{ac}}) \quad (1)$$

With both symmetrical and evenly spaced boundary levels around the input voltage the protection can be triggered equally fast regardless of the polarity of the surge pulse. As is the case with the first implementation, the width of protection margin should be selected carefully so that both a fast response and sufficiently low sensitivity to voltage disturbances are achieved.

2) Two Analogue Comparators with Internal or External Reference Voltage

The use of internal reference voltage is particularly useful in case of the absence of digital-to-analogue converter peripherals within a microcontroller environment.

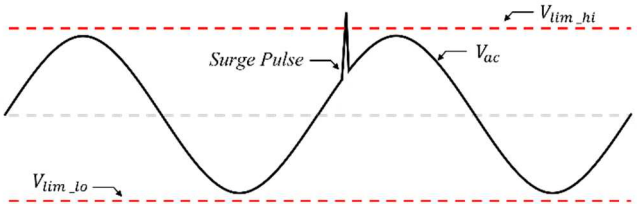

Fig. 7. Alternative voltage boundary forming method using a pair of two comparators with internal reference voltage.

Most of the microcontrollers are embedded with an internal reference voltage which provides a stable output voltage to comparators. In this way, a pair of fixed boundaries can be formed to provide a constant protection level throughout each line half cycle (Fig. 7). However, one must take notice of the limitations using this arrangement since there might only be a few submultiple values of the reference voltage levels to choose from. Otherwise, a different method to provide a fixed reference signal may be required. In addition, the response time from a microcontroller can vary based on the angle at which the voltage transient occurs.

IV. Simulation Implementation and Results

Simulation results are essential to evaluate the current and voltage strength of the power stage at any time of development. To achieve meaningful results, the simulation setup is based on the specifications of EN 61000-4-5 standard. The simulation model is implemented and verified using LTSpice software.

A. Power Inductor Non-linearity

It is often the case that higher voltages can be applied across inductors for short durations without damage. Such voltages may occur in the form of occasional spikes or surge voltages. The capability of a specific inductor to withstand temporary over voltages may be quite high and is not always directly related to the maximum continuous operating voltage rating. The ability to withstand high, temporary, surge voltages depends both on the specifics of the inductor construction as well as the magnitude, rise time, and specific waveshape of the high voltage. The percentage of initial permeability or "roll off" value of the actual inductor is modeled based on the provided manufacturer datasheet [8].

Sendust type of powder core (MS109125-2) is said to have an initial inductance of 500µH and follows the saturation current profile as the initial permeability %μ_i drops with higher DC bias current indicated in Fig. 8 below.

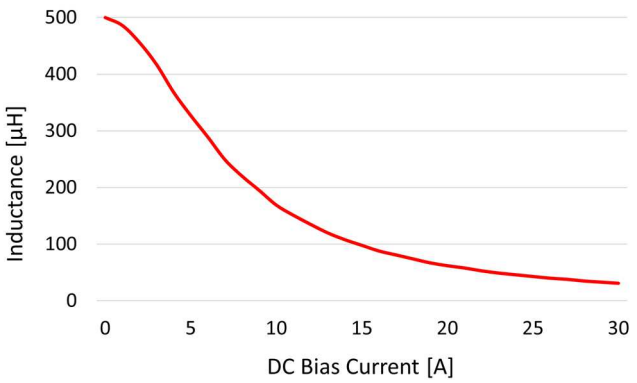

Fig. 8. Inductor vs current curve for Sendust core (MS109125-2).

During a positive half line cycle with duty ratio $D > 0$, voltage applied across the inductor during charging (2) and discharging (3),(4) can be computed as follows:

$$V_L = L\left(\frac{\Delta i_L}{\Delta t}\right) = |V_{ac}| \tag{2}$$

$$V_L = L\left(\frac{\Delta i_L}{\Delta t}\right) = |V_{ac}| - V_{fly} \tag{3}$$

$$V_L = L\left(\frac{\Delta i_L}{\Delta t}\right) = |V_{ac}| - V_{bulk} + V_{fly} \tag{4}$$

Likewise, the flying capacitor C_{fly} is energized and de-energized (5) for the same given period by:

$$\Delta Q = i_L(t)(1 - D)T_{PWM} \tag{5}$$

B. Simulation Parameters

The component values are chosen to be as close to the practical implementation as possible. The system is said to be operating in PFC mode using a closed-loop current mode control. Configuration includes voltage signal $V_{ac} = 230V$ followed by a two-stage mains input filter. Parasitic elements are not considered in detail for the purpose of this simulation. The switching leg devices Q_{1-8} are configured as ideal switches. Each of them are fitted with and additional diode acting as an intrinsic element. Power stage is fitted with a flying capacitor $C_{fly} = 9.4\mu F$, bulk capacitor $C_{bulk} = 1.4mF$ and main inductor $L_{main} = 500\mu H$.

Note that surge pulse amplitude is adjusted down to 290V due to the absence of additional line varistor to absorb surplus energy. The simulation was also carried out using S20K275 (TDK) MOV with a manufacturer provided spice model. However, due to slower convergence and minimal disparity in final simulation results for both methods it is not covered in the later work. 3-level bidirectional BTP inverter simulation waveforms are captured during an input voltage surge at $\phi = 90°$. Input voltage $V_{AC} = 130V$, output voltage $V_{out} = 400V$ and output load $P_{out} = 650W$.

C. Simulation Results

To emphasis the need for a fast surge detection method refer to Fig. 9 below. It is evident that in case of a continuous boost mode operation after input voltage surge only few switching cycles are required before the inductor current is significantly ramped up. The controller cannot react fast enough to compensate for this and in turn can lead to a substantial swing of the flying capacitor C_{fly}. During the time $Q_{3,4}$ and $Q_{7,8}$ are on, flying capacitor gets discharged by (1), however even with large voltage (4) applied across the inductor the current flowing through it is not saturated resulting in only a small FC voltage drift. In contrast, during the flying capacitor charge sequence (5) with $Q_{1,2}$ and $Q_{5,6}$ conducting, inductor current is now saturated. This leads to a significant surplus charge added to the flying capacitor subjecting the composite device $Q_{3,4}$ to more than 300V. Hence, MOSFET devices are bound to operate in what is known as breakdown region with excess drain current I_D.

Captured waveforms are as follows: switch node voltage V_{sw} - (green), input voltage V_{ac} - (yellow), flying capacitor voltage V_{fly} - (blue), main inductor current I_L - (red).

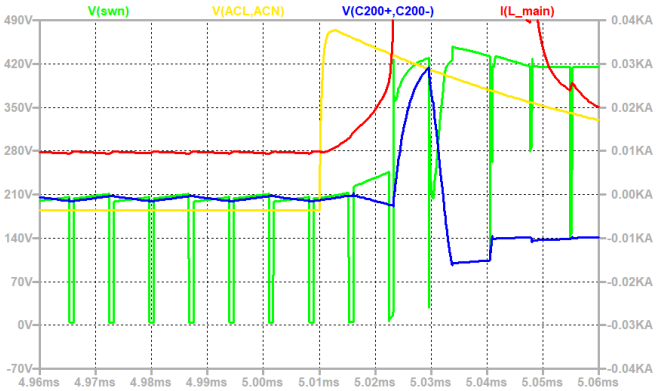

Fig. 9. Input voltage surge with no fast protection and continuous boost mode operation.

In contrast, being able to suppress all gate drive signals fast enough can protect the flying capacitor(s) without allowing for any rapid charge or discharge during post surge switching cycles (Fig. 10). In this particular example all drive signals are disconnected exactly 10µs after the initial surge pulse is generated. Note that the peak inductor current $I_{L(pk)}$ does not exceed 20A before the applied voltage across it drops close to zero. In this particular example the excess energy is handled by the inrush diode D_1 depicted in Fig. 2.

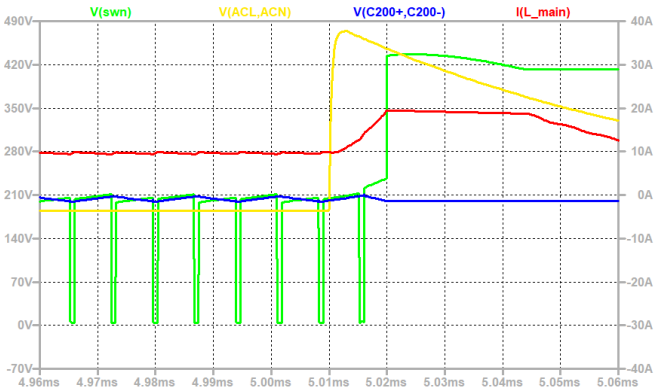

Fig. 10. Input voltage surge with a proposed surge detection method with all gate drive signals turned off 10 µs after initial surge pulse.

V. Experimental Validation

To validate the effectiveness of the proposed surge detection method, the initial surge test procedure and measurements were carried out following the specifications covered in European standard EN 61000-4-5. Bidirectional 1.5kW 3-level BTP PFC/inverter was utilized to obtain waveforms and compare it against the simulation results (Fig. 11).

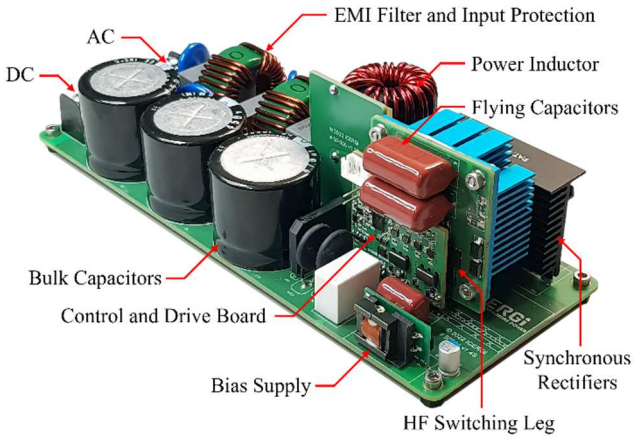

Fig. 11. Bidirectional 1500W 3-level BTP PFC/Inverter hardware prototype.

The converter is fitted with 3 output capacitors $C_{bulk} = 1410\mu F$, PFC inductor $L_{main} = 500\mu H$, flying capacitor $C_{fly} = 9.4\mu F$ and a string of 8 x 150V BSC093N15NS5 MOSFETs. The switching leg is operated with a fixed switching frequency of 65kHz boosting the output V_{bulk} to 400V. Input voltage V_{in} to the system is 130V_{AC} while the output power P_{out} is adjusted to 650W. EM simulator machine is set to output 1500V positive pulse with line-to-line coupling at $\phi = 90°$. Both hardware prototype specifications and experimental setup details are summarized in Table 1 and Table 2 respectively.

TABLE I. Bidirectional Inverter Bill of Materials (BOM)

Component	*Name*	*Description*	*Qty*
Power Stage	C_{bulk}	470µF 450V bulk capacitor	3
	C_{fly}	4.7µF 450V flying capacitor	2
	L_{main}	500µH inductor (MS109125-2)[a]	1
	Q_{1-8}	150V 9.3mΩ MOSFET device	8
	$Q_{SRL/H}$	650V 19mΩ synchronous rectifier	2
Input Protection	MOV_1	430V 8kA varistor (20 mm)[b]	3
	F_1	20A 600VAC/500VDC fuse	1
	GDT	600V 15kA gas discharge tube[c]	1
EMI Filter	C_{X1-2}	1µF 310V_{AC} X – capacitor	2
	C_{X3}	2.2µF 310V_{AC} X – capacitor	1
	C_{Y1-4}	470pF 310V_{AC} Y – capacitor	4
	L_{com1-2}	2mH common mode choke (16A)	2

[a] 2 x 250 µH series connected inductors using 1.5 mm enameled wire

[b] 1 x line-to-line and 2 x line-to-protected earth (B72220S0271K551)

[c] GDT is connected between C_{Y1} and C_{Y2} to PE in a practical system

TABLE II. DUT Specifications and Testing Parameters During Input Voltage Surge

	Parameter	*Name*	*Value*	*Units*
DUT	Input voltage	V_{ac}	130	V
	Output voltage	V_{bulk}	400	V
	Output power	P_{out}	650	W
	Switching frequency	F_{sw}	65	kHz
Surge Module[a]	Surge voltage	V_{surge}	2000	V
	Surge pulse rise/fall	t_r, t_f	1.2/50	µs
	Repetition rate	t_{rep}	15	s
	Phase step	φ_{step}	5	°

[a] UCS 500M4 Ultra-compact simulator

A. Experimental Waveforms

Transitory waveforms of a software based over current protection (OCP) are demonstrated in Fig. 12. It is evident that with a large voltage applied across the inductor the current flowing through it increases rapidly resulting in V_{fly} imbalance during its charging period. Based on a maximum measured switch node voltage V_{sw} it is obvious that output voltage increase is only around 30V from its nominal level of 400V. This implies that based on a switching instant inner MOSFET devices $Q_{3,4}$ or $Q_{5,6}$ can potentially be damaged due to large drain-source voltage blocking. The response time is measured to be around 25µs before the switching action is stopped. Prior to this, the flying capacitor voltage V_{fly} is already charged to around 280V.

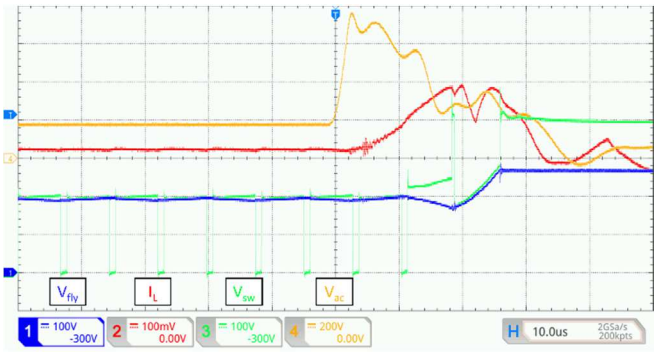

Fig. 12. Input voltage surge waveforms using a software based over current protection. (Inductor current I_L = 20A/div)

The proposed surge detector method is evidently more effective with the measured response time of around 8µs during the same test conditions (Fig. 13).

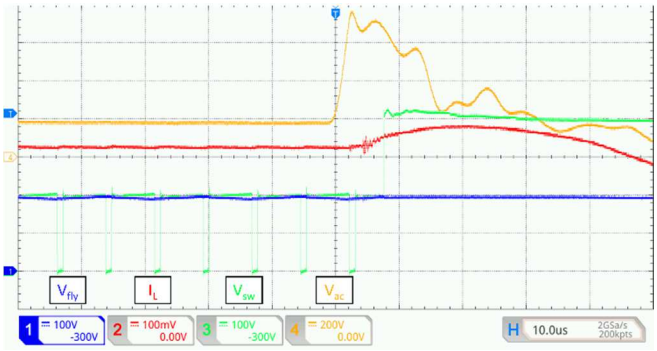

Fig. 13. Input voltage surge waveforms using a proposed surge detection method. (Inductor current I_L = 20A/div)

The microcontroller suspends switching operation fast enough so that the flying capacitor charge remains relatively unchanged. This corresponds to approximately 70% reduction in latency as compared to software triggered OCP. This is particularly of great importance when heavier load conditions as well as higher surge pulses are present. The proposed surge detection method was tested using the same setup up to 1.5kW output load with input voltage surge up to 2000V yielding a similar performance.

VI. Conclusion

In conclusion, the presented work aimed to give a sophisticated overview of the surge detection to prevent the flying capacitor imbalance in FCML converter/inverter applications. The proposed time-efficient and low-cost surge immunity technique is flexible and can be realized on most low-cost microcontrollers available in the market. The proposed surge detection method is not limited to a single type of a converter/inverter and can be easily adopted in higher power rated bidirectional PFC/inverter systems. The experimental data clearly demonstrates the advantageous capabilities of shorter response latency and prevention of the flying capacitor drift during the time a sudden step in voltage is applied across the main inductor.

Some of the technology aspects as well as the implementation details covered in this paper may be subject of patent applications.

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