Feasibility Study of Compact High-efficiency Bidirectional 3-Level Bridgeless Totem-pole PFC/Inverter at Low Cost

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***Abstract*— Bidirectional converters are increasingly being used in electric vehicle chargers and self-consumption for residential/communities with energy-storage capabilities. Among existing bidirectional solutions, bridgeless totem-pole arrangement has been of great interest to both academia and industry due to its advantages of enabling ultra-high efficiency, i.e. above 99%, at low complexity. However, until now most research and development have mainly focused on AC/DC power factor correction (PFC) applications of the bridgeless totem-pole topology with very little effort to understand the practicality and performance of the converter in generation mode, i.e. DC/AC power inversion. Therefore, this article discusses the feasibility of the 3-level bridgeless totem-pole arrangement used as a DC/AC inverter in either islanded or grid-tied operation. This work is experimentally validated by a 3kW bidirectional PFC/Inverter prototype in a compact format of 41mm x 302mm x 1U with peak efficiency exceeding 99% at 230V for all operating modes.**

Keywords—Bidirectional, power factor correction, multi-level, high efficiency, grid-tied inverter, islanded inverter.

I. INTRODUCTION

The bridgeless totem pole topology dates from an early study published by Salmon [1]. The topology has been well-known for its advantages of low conduction loss and component counts. However, its applications only became mainstream recently thanks to increasing market demand for compact and high efficiency power supplies with bi-directional power flow capabilities, such as on-board car chargers and back-up power [2]-[7].

Various studies have looked at detailed implementation and performance evaluation of the bridgeless totem pole topology in PFC rectifier mode using either wide band gap (WBG) devices [2]-[5], or low-voltage MOSFETs in conjunction with multilevel power conversion [6], or super-junction MOSFETs with active snubber [7]. Very little effort to understand the feasibility of the inverter operation has been made in [5]-[7]. Inverter mode control is mentioned briefly in [5], but no experimental evaluation or design details are provided. Although [7] covers an implementation of the bidirectional 2-level totem pole converter in both PFC and islanded inverter mode, it does not discuss any inductor control techniques or EMI challenges associated with power factor (PF) less than 1. Furthermore, the evaluation of the converter performance in [7] is not covered regarding to grid-tied mode.

Therefore, this paper will focus on the feasibility of a bidirectional 3-level converter deployed in either islanded or grid-tied inverter applications.

II. GENESIS OF BIDIRECTIONAL MULTI-LEVEL POWER CONVERSION TOPOLOGY

A bridgeless totem-pole structure proposed in [1] was originally used as a technique for conduction loss reduction. The idea is to replace full bridge rectification in a conventional PFC approach with half-bridge rectification in the totem-pole PFC, allowing removal of one rectifier diode in the power path. Eliminating conduction losses associated with a diode voltage drop typically translates into approximately 1% efficiency gain at low line. Likewise, the conduction loss in the boost stage is reduced due to only active devices present in the switching leg. Recent studies [2]-[6] proposed using high voltage Super Junction (SJ) MOSFETs for implementation of the rectification stage as illustrated in Fig. 1. Such an approach enables even further reduction in conduction loss and bidirectional power transfer which is relevant to self-consumption and EV applications.

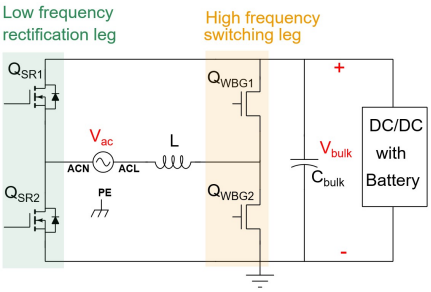


Fig. 1. Conventional bridgeless totem-pole PFC with line synchronous rectification.

The converter as shown in Fig. 1 faces several practical challenges when operated in continuous conduction mode (CCM) with hard switching. Particularly, hard switching transitions rule out usage of Super Junction MOSFETs due to their long reverse recovery time t_{rr} and high reverse recovery charge Q_{rr}. Therefore, the only option left for the implementation of the high frequency (HF) switching leg is Wide-bandgap (WBG) devices, e.g. GaN FETs, SiC FETs. For designers, these devices are currently entering volume production with limited operating history. In addition, WBG devices don't have the same economies of scale as with MOSFET devices due to low volume. A challenging engineering issue with WBG devices is material hard-switching loss confining the operating frequency to less than 100kHz, which results in high volt-seconds product applied

across the inductor. Therefore, the main interest of this study is to develop a new bidirectional topology that can address the following challenges associated with the existing WBG-based implementation:

- Limited packaging standard for GaN components
- High volt-seconds stress on the main PFC inductor. It should be noticed that a volt-second product indicates how much differential EMI noise will be generated by the boost stage. A low volt-seconds product is always desired.

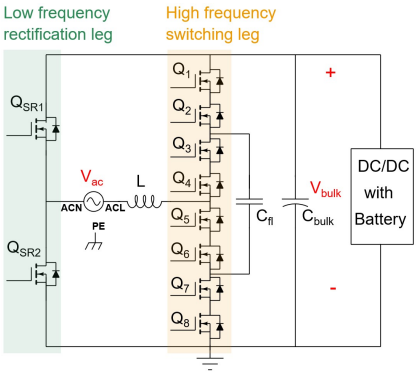


Fig. 2. Bidirectional bridgeless totem-pole 3-level PFC/Inverter.

Fig. 2 illustrates the proposed topology which is similar to that of Fig. 1 except that the conventional HF switching leg is replaced by the 3-level switching leg with a flying capacitor for operating voltage division. The 3-level topology operates with phase cancellation, implying reduced voltage applied to the PFC inductor for shorter amount of time. This innovation enables 4x reduction in volt-seconds product and 2x reduction in operating voltage of switching devices. These features can be translated into:

- 4 x lower differential EMI noise. The PFC inductor could be 4 x smaller or the EMI filters could be smaller or both.
- Enable the usage of 300V Silicon switching devices instead of 600V GaN/SiC FETs. For performance and cost optimization, a 300V-rating composite switch can be implemented by connecting 2 x 150V MOSFETs in series. This explains the reason for 8 x 150V MOSFETs deployed in Fig. 2. Voltage sharing between series connected MOSFETs can be achieved by using the same component type and gate drivers with precise delay matching. Detailed discussions along with an experimental validation could be found in [6].
- Inherently lower dV/dt and dI/dt are of value in limiting EMI/EMC effects.

III. PRINCIPLE OF OPERATION AND CONTROL

A. Modulation Scheme

The directional arrangement of 150V MOSFETs as shown in Fig. 2 suggests that the converter only works if the voltage between the node ACL and local GND is greater than 0V and less than the bus voltage V_{bulk}. This constraint dictates how the rectification leg should be driven. In particular, the low side MOSFET Q_{SR2} is turned on only if the live-to-neutral voltage V_{ac} is positive. Inversely, the high-side MOSFET Q_{SR1} is switched on only if the live-to-neutral voltage V_{ac} is negative. For implementation, certain deadtime is inserted between the drive signals of Q_{SR1} and Q_{SR2} as illustrated in Fig. 3. This practice helps avoid cross conduction in the rectification leg and most issues caused by bumpy transfer around zero crossing points of the AC voltage waveform.

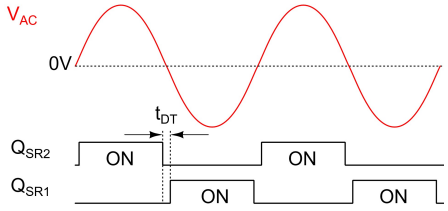


Fig. 3. Modulation scheme for the low-frequency switching leg.

It should be noticed that the drive signals of the two rectifier MOSFETs are modulated based on the AC voltage and not on the AC current. Hence, the modulation technique as demonstrated in Fig. 3 can be applied to both rectification and generation modes of operation.

For reliable operation of the multi-level switching leg as shown in Fig. 2, the voltage of the flying capacitor C_{fl} has to be controlled to follow the reference value of $V_{bulk}/2$ during both transient and steady-steady operation. Several modulation approaches have been proposed in the literature. In this study, phase shift modulation (PSM) is considered due to its benefits of frequency multiplication and natural voltage balance [8].

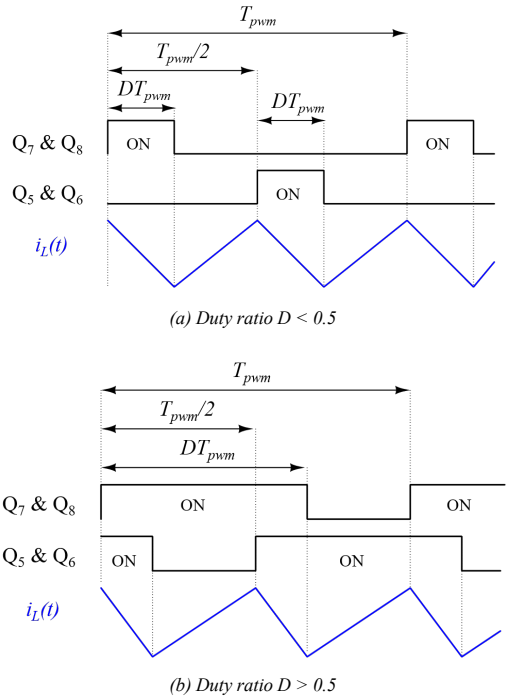


Fig. 4. Exemplary phase-shift modulation and inductor current waveforms of a 3-level flying capacitor converter.

The operation of 8 x 150V MOSFETs in the string can be summarized as follows. Two series-connected MOSFETs of

a composite device, e.g. Q_7 and Q_8 are always driven on and off together. The switching devices in the leg are split into two groups including (Q_1, Q_2, Q_7, Q_8) and (Q_3, Q_4, Q_5, Q_6). Each group will form an operating phase in which components are driven in a complementary manner. When Q_7 and Q_8 are kept on, Q_1 and Q_2 must be kept off and vice versa. Similarly, the drive signals of Q_3 and Q_4 are an inverted version of the drive signals of Q_5 and Q_6. The timing of the drive signals to the MOSFETs Q_5 and Q_6 are a delay version of the drive signals to Q_7 and Q_8. The delay time is a half of the switching period. An example of phase-shift modulation with duty ratio values of above and below 0.5 is illustrated in Fig. 4 where D represents the ratio of the on time of Q_7 & Q_8 to the switching period T_{pwm}. It is evident that the frequency of the inductor current ripple is twice as much as the switching frequency of 150V power devices, confirming the inherent frequency multiplication advantage of the PSM.

Since the PSM scheme as illustrated in Fig. 4 is used in both PFC and inverter implementation, the power flow between the AC and DC sides can be influenced by programming either the inductor current or the duty ratio or both. This feature combined with digital control could greatly benefit bidirectional applications in which seamless transitions from one mode to another are required.

B. Converter Modelling and Control

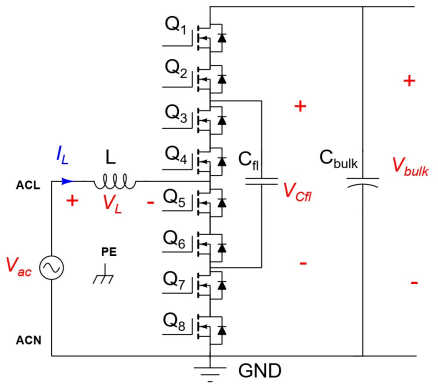


Fig. 5. Equivalent circuit of the proposed bidirectional PFC/Inverter in the positive half cycle of AC line.

In the positive half cycle of AC line, i.e. $V_{ac} > 0$, Q_{SR2} is turned on, connecting the AC neutral to the local ground as illustrated in Fig. 5. It is assumed that

- The MOSFET string is driven by modulated signals with D < 0.5 as shown in Fig. 4
- Converter operates with negligible capacitor voltage and inductor current ripple. In other words, both capacitor voltage and inductor current remain constant within a switching cycle.
- Converter characteristics can be adequately modelled by ideal switches and passive devices.

Given these assumptions, one can derive the large-signal averaged model of the converter during the positive line cycle by following the State Space Averaging (SSA) method as described in [9]. The main result of the analysis is given by

$$L\frac{dI_L}{dt} = |V_{ac}| - (1-D)V_{bulk} \tag{1}$$

where $|V_{ac}|$ denotes the absolute value of AC line voltage. One can easily confirm that (1) is also valid for D > 0.5.
The converter model suggests that the inductor current I_L can be programmed to flow in both directions depending on how the right side of the differential equation (1) is manipulated. In particular, the controller adjusts the duty ratio D in response to variations in AC line, DC bus voltage and inductor current values.

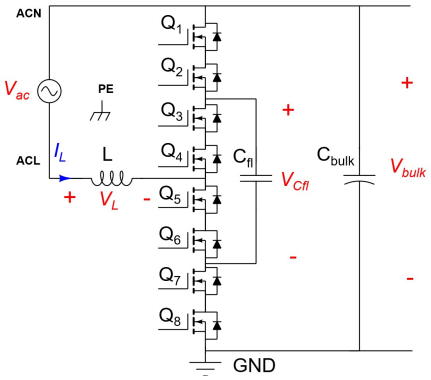


Fig. 6. Equivalent circuit of the proposed bidirectional PFC/Inverter in the negative half cycle of AC line.

In the negative half cycle of AC line, i.e. $V_{ac} < 0$, Q_{SR1} is turned on, connecting the AC neutral to the DC bus as illustrated in Fig. 6. Similarly, the large-signal averaged model of the converter during the negative line cycle can be developed based on the assumptions and SSA approach as mentioned earlier. From a control point of view, the relationship between the inductor current, input voltage and output voltage is again of our main interest. This is governed by

$$L\frac{dI_L}{dt} = -|V_{ac}| + DV_{bulk} \tag{2}$$

Once again, the converter model confirms that bidirectional power flow control is feasible and the controller can use a similar approach to inductor current programing, i.e. duty ratio adjustment according to AC voltage, inductor current, and DC bus voltage.

Comparing the right sides of (1) and (2) shows that the duty ratio D has completely different influence over the way in which the inductor current is programmed in the positive and negative half line cycles. This means that the controller must update its output (assumed to be D), states, and control laws every time the converter changes its operating mode around zero crossing (ZC) of the line voltage. Transition from one control state to another could take dozens of switching cycles. Such a discontinuity in the control signal will distort the inductor current depending on its values around ZC.

The voltage between the power ground and the AC neutral also exhibits steep changes around ZC when synchronous rectification (SR) MOSFETs Q_{SR1} and Q_{SR2} swap their roles. This would result in high common-mode noise and hence complicate EMI filter design as reported in [10]. Noise reduction can be achieved by slowing down the voltage transition at the expense of extra time delay (in the order of 100us) which exacerbates current distortion issues.

Minimal distortion can be observed in a scenario where the inductor current is zero around ZC of line voltage, such as PFC and inverter with a unity power factor (PF). In contrast, significant distortion can be observed in a scenario where the inductor current is maximal around ZC, such as inverter with pure inductive or capacitive loads.

C. Active voltage balancing control

It can be observed in (1) and (2) that the inductor current I_L, and DC bus voltage V_{bulk} or AC voltage V_{ac} can be programmed by varying the duty ratio D. In theory, any variation in D will effectively force the flying capacitor voltage V_{Cfl} to follow the reference value of $V_{bulk}/2$ if natural balance is present. However, natural balance cannot be assured under practical working conditions and transient responses. Furthermore, the natural balancing dynamic could be very slow in some applications depending on the load and capacitance values.

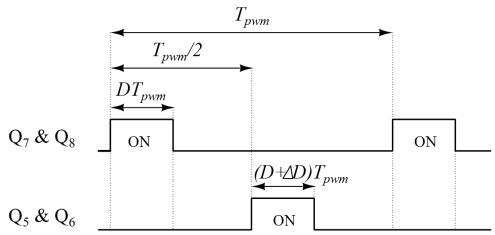


Fig. 7. Enhaced phase shift modulation with an additional variable ΔD allowing full control of the flying capacitor voltage V_{Cfl}.

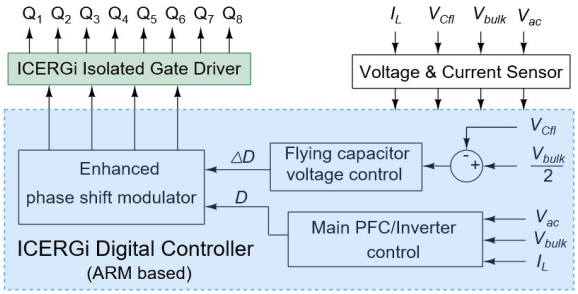
Therefore, it makes sense to introduce another control variable that allows independent control of the capacitor voltage V_{Cfl} regardless of the duty ratio value. This idea could be implemented by enhanced phase shift modulation as proposed in Fig. 7. The primary principle remains the same, making the duty ratio D the main control variable for inductor current and output voltage programming while the flying capacitor voltage V_{Cfl} can be commanded to settle at different points between 0V and V_{bulk} depending on how the variable ΔD is chosen. It should be noticed that ΔD could be set to any value between $-D$ and D; however, only small values of ΔD are required to stabilize V_{Cfl} around the balance point in practice.

IV. VERSATILE HARDWARE PLATFORM

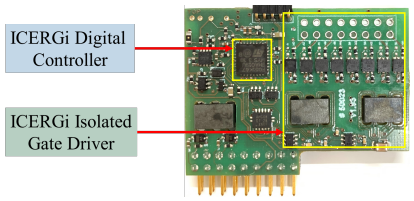
A. Control and Drive

It is desirable to develop a scalable and mappable hardware platform that can be deployed for a wide range of PFC and inverter applications. Such a goal can be achieved by exploiting the benefits of digital control and low-cost isolated gate drive approaches as discussed in [6].

A proposed control and drive solution with enhanced phase shift modulation is illustrated in Fig. 8(a). Firstly, the flying capacitor voltage V_{Clf} can be measured along with other signals, e.g. V_{ac}, V_{bulk}, and I_L using dedicated voltage and current sensors. The outputs of these sensing circuitry will be sampled by the analog-to-digital (ADC) conversion modules of the micro-controller and can be used later for different control purposes. In particular, V_{Cfl} can be input to the flying capacitor controller responsible for calculating the value of ΔD while the main PFC/Inverter control function can update D reflecting the changes in V_{ac}, V_{bulk}, and I_L. The outputs of both the voltage balancing controller and the main PFC/Inverter controller will be fed to the enhanced phase shift modulator which generates PWM control signals according to Fig. 7. The isolated gate drive circuit helps to deliver the PWM signals to the gates of 150V MOSFETs in the switching leg.



(a) Block diagram of ICERGi digital control & drive solution



(b) Compact hardware implementation in 27mm x 37mm

Fig. 8. Integrated drive and control card designed for multiple deployments of the proposed bidirectional 3-level converter.

The control architecture as proposed in Fig. 8(a) offers significant flexibility in product development. For instance, the main PFC/Inverter control block can be updated with different algorithms for different deployments. This point will be exemplified in Sections V and VI.

The ICERGi drive technology as presented in [6] allows driving of multiple switching devices with low component count at low cost by obviating the need for local power supplies as typically required by commercial isolated driver ICs. This self-powering feature enables compact implementation of the proposed drive and control architecture. For example, the ARM M0-based digital controller and 8 isolated drivers can be easily housed in a compact low-cost daughter board as demonstrated by Fig. 8(b). The digital controller can be flashed with different sets of firmware for different end applications, e.g. PFC, grid-tied inverter, etc... This approach has allowed the inherent advantages of multilevel technologies to be realised in a practical and cost-effective fashion at relevant power levels, typically the 300W→3kW range as needed for most of the single-phase AC/DC and DC/AC marketplace.

B. Power stage design

It will be recognized that the circuit diagram as depicted in Fig. 2 has been simplified for ease of presenting and understanding. The following circuits must be included in order to assure reliable operation of the design in practice

- Inrush current during start-up can be managed by placing an NTC thermistor between the AC Neutral and the mid-point of the rectification leg. The thermistor will be bypassed by a relay during steady state to avoid excessive conductor loss. Bypass diodes are also required to provide an alternative low impedance path to the bulk capacitor C_{bulk}, preventing inrush current from going through the inductor L and MOSFET string during startup or AC surge events.
- Flying capacitor C_{fl} needs to be pre-charged to the reference level of $V_{bulk}/2$ before MOSFETs start switching. This can be realized by a diode clamp circuit as proposed in [11].
- Conducted EMI noise generated by PFC/Inverter stages must comply with class B limits as defined in IEC 61000-3-2. Therefore, two-stage filtering is implemented at the input of the bidirectional converter as illustrated in Fig. 9. It provides sufficient attenuation for both differential mode (DM) and common mode (CM) noise.

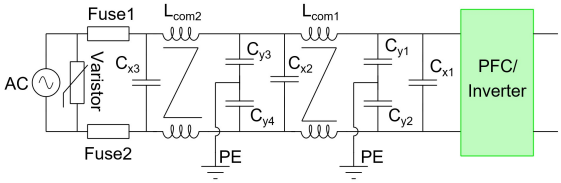


Fig. 9. Two-stage EMI filter with dual fusing and a varistor for surge protection.

A prototype is designed to meet specifications as listed in TABLE I.

TABLE I. BIDIRECTIONAL CONVERTER DESIGN SPECIFICATIONS

Universal line voltage, V_{line}	$85V_{ac} – 265V_{ac}$
Nominal DC bus voltage, V_{bulk_nom}	$400V_{dc}$
Switching frequency, f_{pwm}	66kHz
Maximal real power, P_{max} (rectifer mode)	3kW @ $230V_{ac}$ 1.5kW @$115V_{ac}$
Maximal apparent power S_{max}, (inverter mode)	3kVA @ $230V_{ac}$ 1.5kVA @$115V_{ac}$
Maximal pk-pk flying capacitor voltage ripple ΔV_{fl}	20V
Maximal pk-pk inductor current ripple ΔI_L	3.2A

TABLE II. POWER STAGE BUILD OF MATERIAL (BOM)

Main inductor L= 384uH	2 x 125u permeability Hi-flux core, 35 turns of 1.5mm diamter enamelled wire
Bulk capacitor C_{bulk}	3 x 330uF 450V Electrolytic
Flying capacitor C_{fl}	4.7uF 450V Film // 440nF 450V Ceramic
Switching leg	8 x 150V 11mR MOSFET BSC110N15NS5 in 5mm x 6mm package
Rectification leg	2 x 650V 23mR MOSFET FCH023N65S5 TO247
EMI filter	3 x 1uF 310Vac X- capacitor 2 x 4.4mH common mode choke 4 x 470pF 310Vac Y- capacitor
Bias supply	5W quasi-resonant flyback converter

The analytical procedure as documented in [12] provides a practical engineering tool to design components for the power stage that can satisfy the worst-case operating conditions. An exemplary design is summarized in TABLE II. Fig. 10 shows complete hardware implementation including a control drive card, a 2-stage EMI filter and a 5W bias supply.

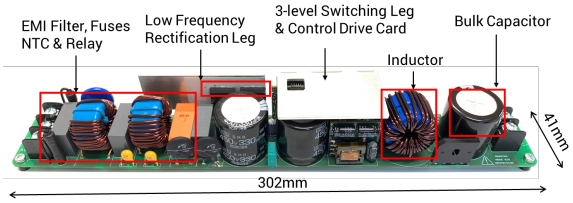


Fig. 10. Bidirectional 3kW PFC/Inverter hardware prototype with a compact inductor and an EMI filter stage. The whole design is confortably fit in a small footprint of 41mm x 302mm x 1U.

V. BIDIRECTIONAL PFC/GRID-TIED INVERTER DEPLOYMENT

One exemplary deployment of the proposed bidirectional PFC/Inverter converter is to use as the front-end stage of an on-board electric vehicle (EV) charger. The power flow can be controlled to either charge up the EV battery pack during quiet time or return energy to the grid during peak time. This feature enables new opportunities in achieving flexible power management for grid distribution networks. In particular, beyond the historical intention as a passive load to the utility network, EVs now can serve as distributed energy storage with grid support capabilities.

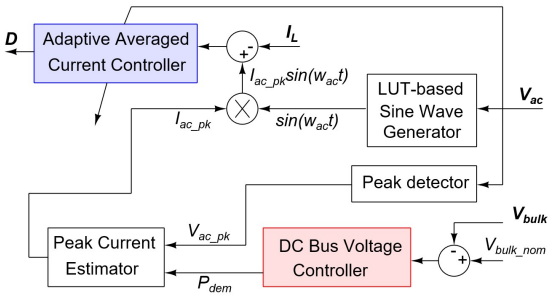


Fig. 11. Block diagram of unified PFC/grid-tied inverter control algorithm.

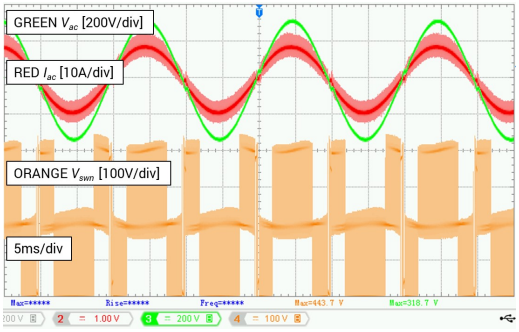
Since the grid voltage and frequency are regulated by the electricity network operator, inverters can interact with the grid only through current injection. The grid-tied inverter mode is assumed to generate real power only. In other words, the current injected to the electricity network will follow the wave shape of the AC line voltage but they will be 180 degrees out of phase. This is exactly the opposite of what PFC functionality is supposed to be. So, it is expected that a single controller could effectively benefit both the PFC and grid-tied inverter modes.

Fig. 11 exemplifies a unified approach to PFC/grid-tied inverter control in which the averaged DC bus voltage will be regulated around the nominal voltage V_{bulk_nom}. For PFC applications, the energy will flow out of the DC port, naturally bringing the averaged DC voltage below V_{bulk_nom}. The voltage controller will regulate the DC bus by commanding positive demand power, i.e. $P_{dem} > 0$. Such a command will translate into positive demand peak AC

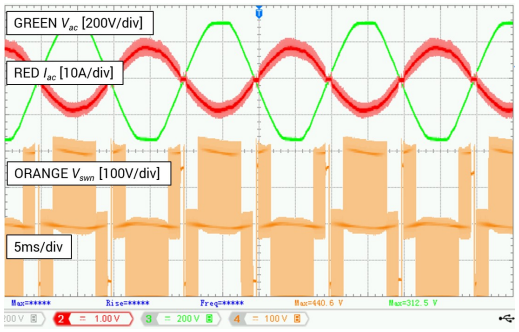
current, i.e. $I_{ac\_pk} > 0$. The sine wave generator is implemented by a look-up table (LUT) with an AC voltage input for phase synchronisation. The output of the generator - a pure sine wave in phase with the AC line voltage - is multiplied with I_{ac_pk} to provide the reference $I_{ac\_pk}sin(wt)$ for inductor current programming. Since I_{ac_pk} is positive, the current reference should be in phase with the line voltage. This confirms that the power flow will be from the grid to the AC port of the converter.

The controller will behave in a reverse manner for grid-tied inverter operation in which the energy will flow from the battery into the DC port, lifting the averaged DC voltage above V_{bulk_nom}. Regulating the DC bus in this case will result in negative demand power, i.e. $P_{dem} < 0$ and consequently negative demand peak AC current, i.e. $I_{ac\_pk} > 0$. Since the sign of I_{ac_pk} is changed, the current reference will be out of phase with the line voltage. This defines a reverse power flow, i.e. from the AC port to the grid. Owing to space constraint, some protection features related to inverter mode, e.g. anti-islanding operation detection, are not included in this paper.

As mentioned in Section IV.A, the control algorithm as shown in Fig. 11 is an example how the PFC/Inverter control block in Fig. 8(a) can be implemented.



(a) In PFC mode with 230Vac input and 1.5kW load



(b) Grid-tied inverter mode with nominal DC of 400V and 1.5kW

Fig. 12. Operating waveforms of the bidirectional 3kW PFC/Inverter prototype

Fig. 12 (a) and (b) present experimental voltage and current waveforms captured at nominal line voltage of 230V_{rms}, nominal DC bus voltage of 400V, and a power level of 1.5kW in PFC and grid-tied inverter modes, respectively. For PFC measurements, the AC input is provided by a programmable AC source while the inverter mode of operation uses the grid voltage. The switched node voltage shows steps of 200V which is well within the aggregate voltage rating of two series-connected MOSFETs. Fig. 12 also highlights that the converter operates in a stable manner with no sign of voltage imbalance, confirming the robustness of active voltage balancing control.

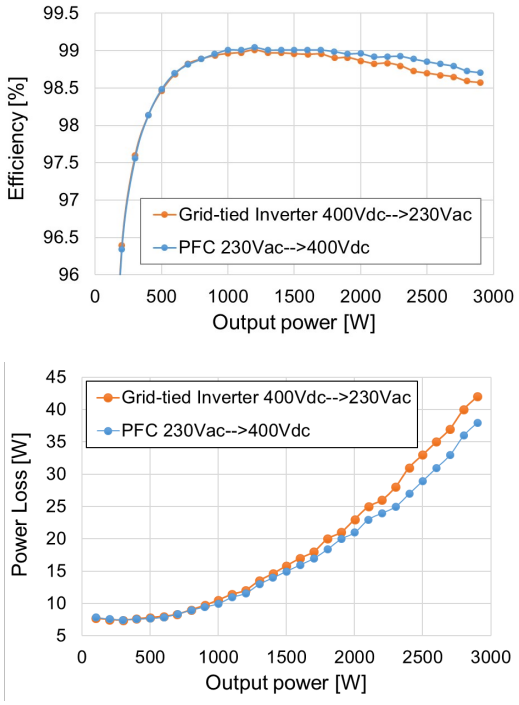


Fig. 13. Power stage fficiency and power loss measured in both PFC and grid-tied inverter.

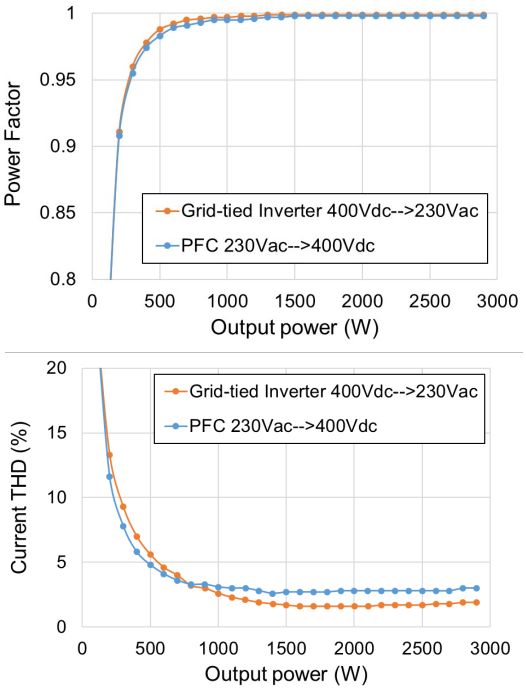


Fig. 14. Power factor and current THD measured in PFC and grid-tied inverter modes of operation

Fig. 13 presents the efficiency and the total losses of the bidirectional converter operating in PFC and grid-tied inverter modes with a 100W step load. The efficiency peaks around 99% at 230Vac for both modes. Both efficiency curves are relatively flat and show very little roll-off at full power.

The digital controller has a current loop that is designed to adapt its gain depending on inductance values. This helps to maximize the control bandwidth without compromising system stability. The outcome is close-to-unity power factor, i.e. above 0.99, and low current distortion, i.e. below 5% for 500W-3kW loads as demonstrated in Fig. 14. High PF and low AC current distortion are observed in both operating conditions. This ties in very well with the discussion in Section III.

VI. BIDIRECTIONAL PFC/ISLANDED INVERTER DEPLOYMENT

For some bidirectional PFC/Inverter deployments, the energy stored in the battery pack may be used to power circuits that are detached from the grid forming an "island". Such an inverter mode is typically referred as islanded operation. An exemplary application is battery storage with bidirectional chargers. One direction is utilized to charge the battery with the power from the grid while operating in the other direction allows powering electronic equipment or tools, e.g. vacuum cleaners, AC motors, using the storage energy.

Unlike the grid-tied mode, islanded inverters must be able to regulate AC frequency and voltage with a proper control. This indicates that the control algorithm developed for grid-tied operation in Section V cannot be used, and unifying controllers for both PFC and islanded inverter modes is infeasible. A solution is to have two separate control blocks, one is for PFC and the other is for islanded inverter. Switching from one operating mode to the other can be implemented via communications or a selectable signal.

The control method for PFC will be similar to that as illustrated in Fig. 11 except for the demand power P_{dem} which is limited to positive values only. Experimental waveforms and performance will also be similar to those discussed in Section V; therefore, the focus of this section will be on control design and validation for islanded inverter.

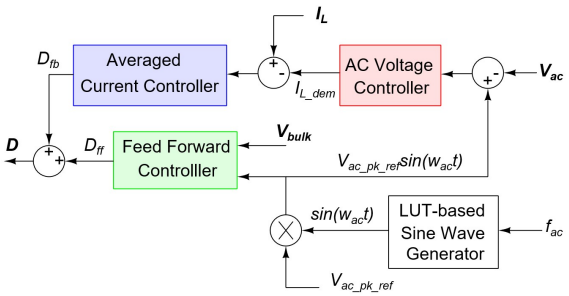


Fig. 15. Proposed control solution for islanded inverter operation

The control objective is to generate a pure sinusoidal voltage with programmable amplitude and frequency. A well-known approach in the literature is to use a look-up table for reference signal generation and a feed forward controller for duty ratio calculation. Even though this open-loop controller is quite stable, it doesn't take into account load variations and component tolerance, which may result in significant distortions in generated AC voltage waveforms for high operating current.

The voltage distortion issue can be addressed by enhancing the open-loop controller with a feedback path as demonstrated in Fig. 15. Any discrepancy between the reference $V_{ac\_pk\_ref}sin(wt)$ and the measured AC voltage will be fed to the AC voltage controller followed by the current controller. The output of this feedback loop is D_{fb} which is intended to minimize the voltage discrepancy. The usage of inductor current information enables better noise immunity and faster control loop bandwidth.

The formulae for the feed forward controller can be simply expressed by

$$D_{ff} = \begin{cases} 1 - \dfrac{\left|V_{ac\_pk\_ref}\sin(wt)\right|}{V_{bulk}} & if \quad V_{ac\_pk\_ref}\sin(wt) > 0 \\ \dfrac{\left|V_{ac\_pk\_ref}\sin(wt)\right|}{V_{bulk}} & if \quad V_{ac\_pk\_ref}\sin(wt) < 0 \end{cases} \tag{3}$$

Transitions from positive to negative AC half cycles and vice versa are implemented to happen instantaneously. This helps to minimize the inductor current distortion around ZC of the AC voltage at the expense of higher common mode EMI noise.

Fig. 16 shows the AC voltage and current supplied to a pure 1.5kW resistive load by the islanded inverter. The programmed voltage level is set to be 230Vrms. Since the inductor current is close to zero around ZC of the AC voltage, it should be expected that a minimal distortion can be achieved.

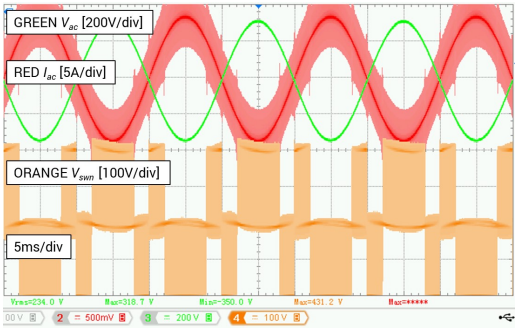


Fig. 16. Operating waveforms of the bidirectional converter captured in islanded inverter mode with a resistive load at Vac = 230Vrms and 1.5kVA

Fig. 17 illustrates another testing condition where the pure resistive load is replaced with a capacitive load. The load current is 90 degrees out of phase with the AC voltage. One can easily notice that the capacitive load current is disrupted around ZC of the AC voltage. This is expected as the controller has to update its states in response to disruption in the converter gain before and after ZC.

Fig. 18 presents testing waveforms with an inductive load. The nonlinearity observed in the current waveform is due to inductance roll off. The load current in this case is

also 90 degrees out of phase with the AC voltage. Since the inductive load current cannot be disrupted, any variation in the converter inductor current will be absorbed by the X-rated capacitors which explains the reason for AC voltage fluctuations after ZC.

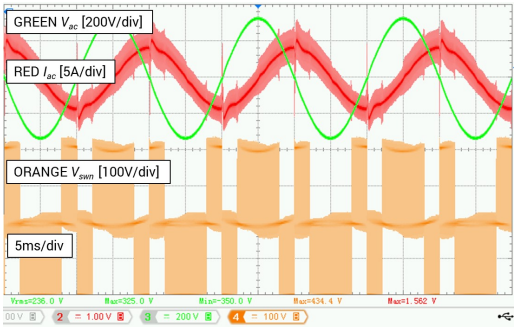


Fig. 17. Operating waveforms of the bidirectional converter captured in islanded inverter mode with a capacitive load at Vac = 230Vrms and 1.5kVAr

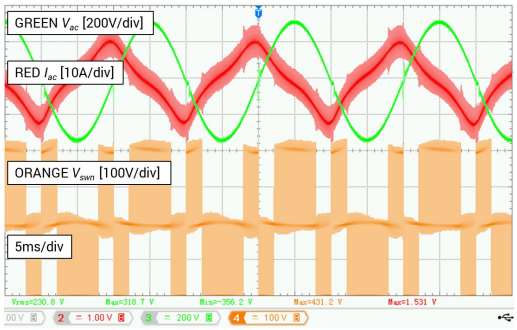


Fig. 18. Operating waveforms of the bidirectional converter captured in islanded inverter mode with an inductive load at Vac = 230Vrms and 1.5kVA

VII. CONCLUSIONS

Bridgeless totem pole topologies are well suited for bidirectional PFC/Inverter applications. Multilevel solutions also have sustainable competitive advantage in magnetics size (four-time reduction) and EMI/EMC performance, as well as an expected long-term cost and performance advantage over conventional (2-level) WBG (SiC and GaN) -based realizations.

The study demonstrates that the discontinuity in the converter gain and EMI related soft transition delays around ZC have significant impact on inductor current distortion unless the current values are close to zero as typically associated with a unity or close-to-unity PF. For applications with a PF less than 1, inductor current distortion around ZC is unavoidable and several techniques such as using faster controllers with adaptive gain or removing soft transitions at the cost of greater EMI can be deployed to alleviate the issue. The study also confirms that established low-cost 150V silicon MOSFETs can achieve better than 99% efficiency in bidirectional 3-level PFC/Inverter.

Many of the techniques discussed in this paper have parallel deployments in DC/AC and general energy management. These topics will be discussed in a future article.

Some of the technology and implementation details presented in this paper were patented while others may be subject of ongoing patent applications.

REFERENCES

[1] J. C. Salmon, “Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage output”, in *Proc. IEEE Applied Power Electron. Conf.*, Mar. 1995, pp. 437-479

[2] L. Zhou, Y. Wu, J. Honea, and Z. Wang, “High-efficiency true bridgeless totem pole PFC based on GaN HEMT: Design challenges and cost-effective solution”, in *Proc. Power Conversion Intelligent Motion Conf.*, May 2015, pp. 1482-1489

[3] S. Dusmez, and Z. Ye, “Designing a 1kW GaN PFC stage with over 99% efficiency and 155W/in^3 power density”, in *Proc. IEEE Workshop on WBG Power Devices and Applications.*, Nov. 2017, pp. 225-232

[4] GaN Systems. (2019). High Efficiency CCM Bridgeless Totem Pole PFC Design using GaN E-HEMT. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/09/GS665BTP-REF-rev180905.pdf

[5] Y. Tang, W. Ding and A. Khaligh, "A bridgeless totem-pole interleaved PFC converter for plug-in electric vehicles," in Proc. IEEE *Applied Power Electron. Conf. and Expo. (APEC)*, Mar. 2016, pp. 440-445

[6] T. T. Vu and E. Mickus, "99% Efficiency 3-Level Bridgeless Totem-pole PFC Implementation with Low-voltage Silicon at Low Cost," IEEE *Applied Power Electron. Conf. and Expo. (APEC)*, Mar. 2019, pp. 2077-2083.

[7] B. T. Irving, Y. Jang, and M. M. Jovanovic, “Implementation and performance evaluation of 100kHz, soft-switching bidirectional PFC/Inverter with silicon MOSFETs”, in Proc. IEEE *Applied Power Electron. Conf. and Expo. (APEC)*, Mar. 2018, pp. 1989-1995

[8] T. A. Meynard, and H. Foch “Multilevel conversion high voltage choppers and voltage-source inverters”, in *Proc. IEEE Applied Power Electron. Conf.*, Mar. 1993, pp. 168-174

[9] Erickson, R. W. and Maksimovic, D. *Fundamental of power electronics*, 2nd Edition, Kluwer Academic Publishers, 2001

[10] B. Zhang, K. Shi, Q. Lin, G. M. Dousoky, M. Shoyama and S. Tomioka, "Conducted noise reduction of totem-pole bridgeless PFC converter using GaN HEMTs," 2015 IEEE International Telecommunications Energy Conference (INTELEC), Osaka, 2015, pp. 1-5.

[11] T. T. Vu, and G. Young, “Implementation of multi-level bridgeless PFC rectifiers for mid-power single phase applications”, in *Proc. IEEE Applied Power Electron. Conf.*, Mar. 2016, pp. 1835-1841

[12] ICERGi, “3kW Bidirectional PFC/Inverter Power Stage Design and Loss Analysis”, Application Note AN007, unpublished