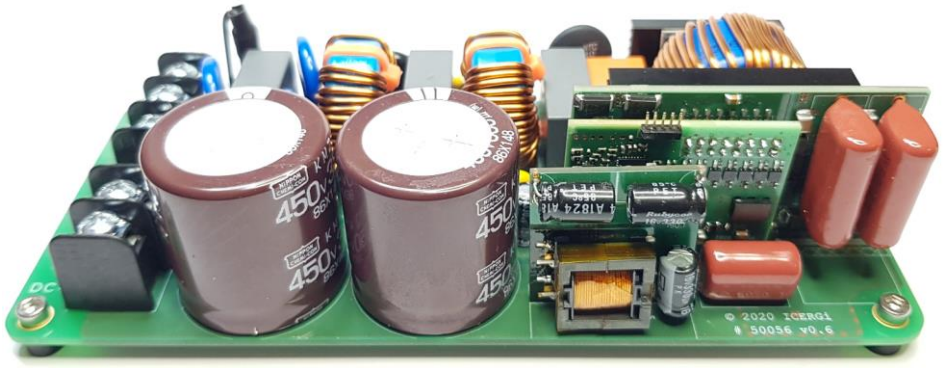
Universal 9A-Input (2000W) Totem-Pole PFC Test Report



- High efficiency
  98.8%* | 97.6%
- Power density
  75W/in^3
- Cost and complexity
  Low

* 99% with a synchronous rectification

About this document

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This document covers both the user manual and the test report of the universal 9A-input bridgeless totem-pole boost PFC evaluation board. It provides the in-house carried out test results, followed by the list of the necessary equipment used to complete them. Relevant waveforms are supplied to indicate the behaviour of the system under certain test conditions. In addition, general guidelines and other important information on “how to use the system” are supplied where necessary too. It has been prepared and published by the ICERGi test and design team members to provide a technical assistance for qualified technical staff. This document should be carefully read to ensure that the provided equipment is correctly implemented before any tests are performed for the sake of minimizing any safety hazards and increasing reliable performance of the system.

Important notice

All specifications and test results of the equipment as well as other details provided in this document are believed to be correct at the time of publishing.

ICERGi evaluation boards and reference boards as well as the information provided in this document are intended to assist qualified and skilled technical staff only for laboratory usage and shall be used and managed according to the terms and conditions set in this document and other supplementary documentation provided with the corresponding equipment. ICERGi has not conducted any testing other than that specifically described in the published documentation for a particular reference design. Evaluation and reference boards provided by ICERGi are subject to functional testing only under typical load conditions.

The evaluation and reference boards are not commercialized products and are solely intended for evaluation and testing purposes. In particular, they should not be used for reliability testing or production. The evaluation boards and reference boards may therefore not comply with CE or similar standards and may not fulfill other requirements of the country in which they are operated by the client. The client must ensure that the equipment received from ICERGi will be handled in a way which is compliant with the relevant requirements and standards of the country in which they are operated.

It is the responsibility of the client’s technical departments to evaluate the suitability of the evaluation and reference boards for the intended application and to evaluate the completeness as well as correctness of the information provided in this document with respect to such application.

ICERGi reserves the right to make corrections, enhancements, improvements and other changes to its evaluation board designs and other items without any further notice.

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If you are unable to agree to these terms and conditions, please return the equipment to ICERGi prior to any evaluation and we shall refund the shipping cost. In case of any questions or doubts, clarify it from the ICERGi company first and then proceed further. Both the email and the website address can be found at the bottom of each page.

Safety precautions

Warning: The DC link of this particular evaluation board can reach up to $400V_{DC}$. In case of measuring waveforms with an oscilloscope, high-voltage differential probes are required. Failure to do so can lead to a personal serious injury or even death.

Warning: The evaluation board contains DC electrolytic bulk capacitors which take time to discharge after the main supply is removed and/or the load is disconnected. Prior to handling of the system, give a sufficient amount of time for the capacitors to discharge to safe voltage levels. Failure to do so can lead to a personal serious injury or even death.

Warning: During testing the evaluation or reference board is connected to an AC grid voltage. For this reason, high-voltage differential probes are required when an oscilloscope is used to capture waveforms. Failure to do so can lead to a personal serious injury or even death.

Warning: Remove or disconnect power from the evaluation or reference board before disconnecting or reconnecting wires or conducting maintenance work. Wait a sufficient amount of time after removing the power in order for the DC bulk capacitors to discharge to zero potential. Failure to do so can lead to a personal serious injury or even death.

Caution: Heatsinks and other component surfaces of the evaluation or reference board may be subjected to hot temperatures during testing. Therefore, necessary precautions are required while handling the board. Failure to do so may lead to a personal injury.

Caution: Only qualified technical personnel that are familiar with power electronics and other associated machinery should plan, install and deploy the system for evaluation purposes. Eye protection and other available protective gear must be worn at all times during the testing of a system. Failure to comply may result in a person getting injured and/or damaging the equipment.

Caution: An incorrect installation of a Digital Power Module consisting of control and power boards can compromise the intended functionality of the evaluation or reference board as well as the damage of components. Wiring or other applications errors such as excessive ambient temperature can lead to the malfunctioning of the system.

Caution: The evaluation or reference board may be shipped in a protective packaging and must be removed prior to installation and testing. Moreover, it may contain additional equipment that must be used appropriately. Failure to remove all packaging and/or use additional equipment appropriately could result in system overheating or abnormal operating conditions.

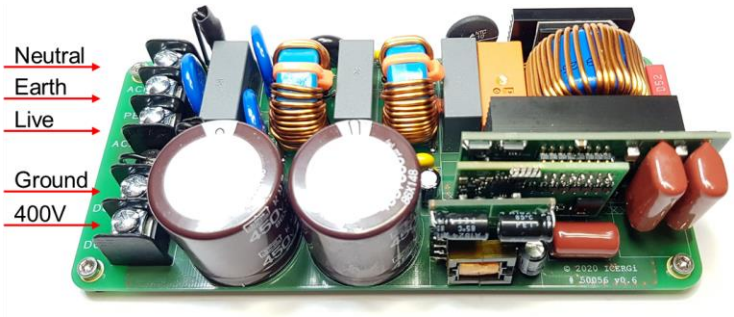
Installation notes

- Contents of the box
  - 1 x Open frame 9A-Input (2kW) PFC evaluation board
  - 1 x San Ace 40 9GV0412J301 12V Fan

- Connections

Input voltage range should not exceed the limits of ($85V_{AC}$ – $265V_{AC}$).

Ensure that the heatsink attached to a diode bridge rectifier is connected to the protected earth (PE) as well as the heatsink of the digital power module which should be tied to a local ground.



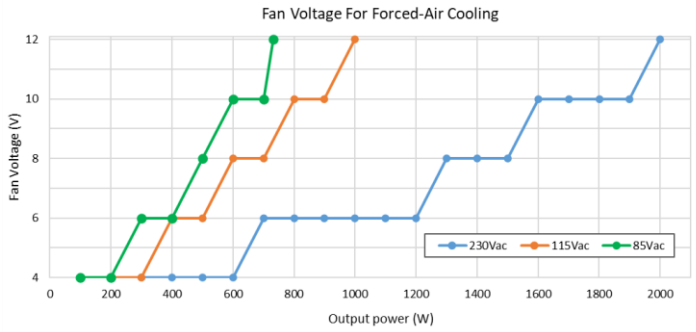
- Cooling

The evaluation or reference board requires a forced air cooling to deliver the rated power.

A standard 1U 12V fan with a similar air flow rating to the one that is provided in the box (San Ace 40 9GV0412J301) is recommended to be used.

The fan should be placed as close to the board as possible. The recommended fan position and the airflow direction are illustrated on the right.

An external DC power source is required to drive a fan. In addition, the airflow of the fan should be controlled manually while adjusting the voltage level that corresponds to the output load and the input voltage to the system as illustration on the right.



- Protection

The evaluation or reference board is fitted with both live (L) and neutral (N) line PTH slow-blow fuses. It is recommended to check if the circuit is not open on the input side to the system prior to the start-up.

Loading the evaluation or the refence board during the time the PFC controller is powered off (latch-up mode, etc.) for a prolonged period of time (> 2 minutes), could lead to the overheating of the NTC device. This can result in the damage of components and subsequent system failure. It is recommended to unplug or disconnect the output load when the PFC stage enters latch-up mode. This can occur only during the standalone PFC stage testing and should not happen in the case of a complete system consisting of an additional downstream stage.

- Power-up

Before powering up the system, please refer to the *Safety precautions* section. The evaluation or the reference board must be installed correctly in a controlled environment which restricts access to any un-authorised personnel.

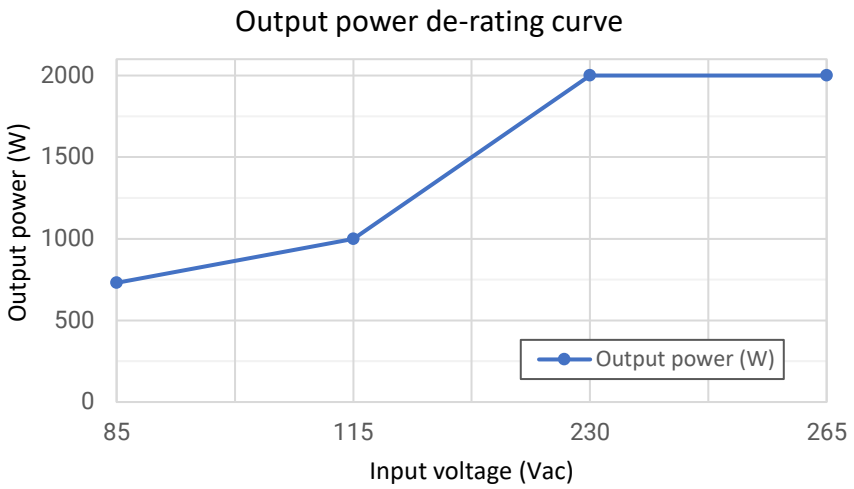
It is recommended to use measurement instruments such as a digital multimeter (DMM) or an oscilloscope, etc. to ensure that the system is operating correctly.

- De-rating

Remember to take the appropriate de-rating into consideration before/during the time the system is powered on.

The output power of the system must be de-rated while adjusting the input voltage by approximately 9W/V_{RMS} below 230V_{RMS}.

- P_{OUT} = 2000W @ V_{IN} = 230V_{RMS}
- P_{OUT} = 1000W @ V_{IN} = 115V_{RMS}
- P_{OUT} = 730W @ V_{IN} = 85V_{RMS}



- Servicing

The evaluation or the reference board contains no additional replacement parts. In case of any repairs, it should only be carried out by authorised technical personnel. If there are uncertainties with regards to this matter, please contact ICERGi for further information.

- Testing

The test setup will depend upon the type of test that is being performed. To verify or characterize the performance of the reference design various measurement instruments such as DMM, oscilloscope, power analyser, etc. are required. The list of recommended equipment required to carry out these tests are provided in *Section 2*.

- Other

Inspect the reference unit for any damages. Units can sometimes arrive defective/faulty due to transit. In case of the transit damage, DO NOT attempt to connect power to the unit. Instead, contact us for an alternative solution.

Ensure that the appropriately sized cables and connectors are used. If needed, use an additional cable support to reduce stress on connectors.

Contents

1. PFC technology overview

The reference design covered in this test report is the universal 9A-input bridgeless totem-pole boost power factor correction (PFC) developed and implemented using ICERGi proprietary gate drive technology as well as the control approach. The PFC stage block diagram is demonstrated in Figure 1 as well as the high-level circuit diagram as per Figure 2.

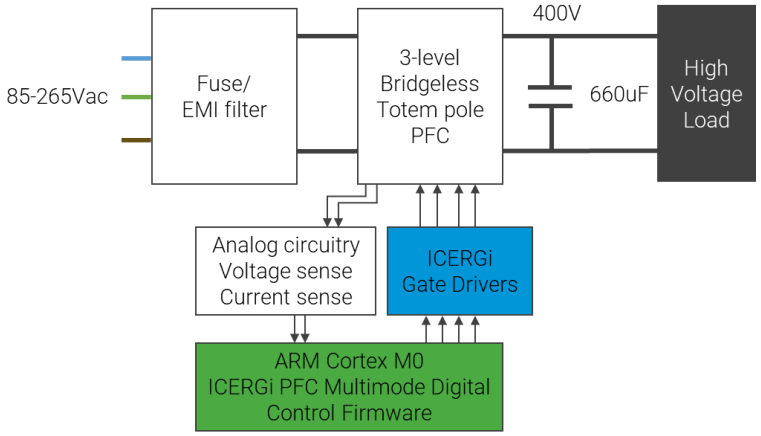


Figure 1: Block diagram of the ICERGi boost PFC stage

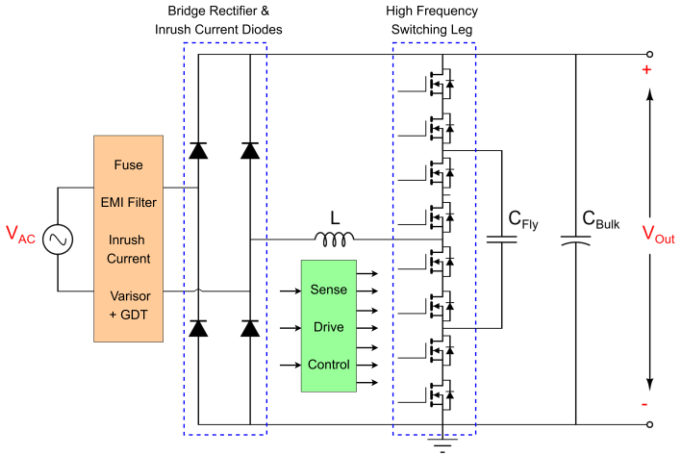


Figure 2: Circuit diagram of a 3-level bridgeless totem-pole PFC

Figure 3 indicates key hardware components of the PFC evaluation board followed by a summary of electrical specifications in Table 1.

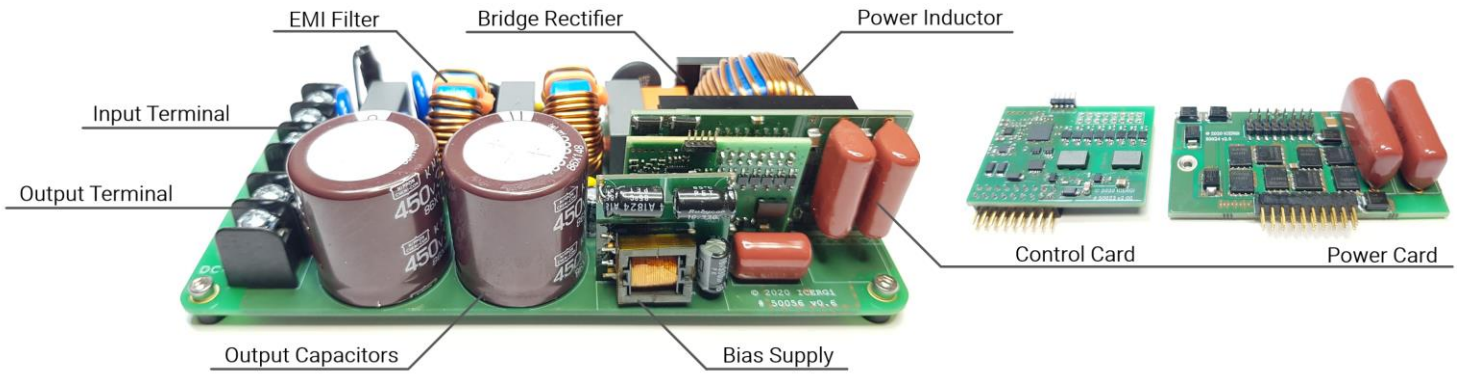


Figure 3: Universal 9A-input PFC evaluation board

Table 1: Electrical specifications of the evaluation board

	Description	Electrical specifications
Input	Voltage range	$90V_{AC}$ – $265V_{AC}$
	Maximal current	$9A_{RMS}$
	Frequency range	47Hz – 63Hz
Output	Nominal voltage	$400V_{DC}$
	Maximal output current	$5A_{RMS}$ at V_{IN} = $230V_{AC}$, $2.5A_{RMS}$ at V_{IN} = $115V_{AC}$
	Maximum power	1000W at $115V_{AC}$, 2000W at $230V_{AC}$
Bias	Nominal voltage	$12V_{DC}$ (± 5%)
	Maximum power	N / A

NOTE: this document does not provide a full specifications data. Instead, refer to a datasheet that is provided in a separate document.

2. Test equipment

Table 2 provides a full list of the in-house test equipment used to evaluate the PFC board. Both the equipment and the test setup details are included in different test routines where applicable.

Table 2: List of the in-house test equipment

No.	Equipment	Manufacturer	Model No.
1	Digital Multimeter	Brymen	BM869s
2	Power Quality Analyzer	Tektronix	PA1000
3	DC Electronic Load	EA Elektro-Automatik	EA-EL 3400-25
4	Spectrum Analyzer	Rigol	DSA815
5	Ultra-compact EM simulator	EM Test	UCS500-M4
6	Line Impedance Stabilization Network	Rohde & Schwarz	HM6050-2
7	Digital Storage Oscilloscope	Rigol	DS4014
8	AC/DC Current Clamp Meter	Pico Technology	TA189
9	Differential Oscilloscope Probe	Pico Technology	TA043
10	Differential Oscilloscope Probe	Testec	TT-SI-51
11	Variable Autotransformer	Alde Tronics	VA-50
12	Isolation Transformer	Triad Magnetics	VPM240-20800
13	Tapped Auto Transformer	EM Test	V4780
14	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ
15	Thermal Imaging Camera	FLIR One	435-0002-02-00
16	Programmable AC Source	Keysight	AC6801A
17	DC Fan	Sanyo Denki	SanAce 40

3. Performance and steady-state operation

This chapter presents the performance and behaviour of the universal 2 kW (9A-input) boost PFC evaluation board during a steady-state mode of operation.

3.1 Test specifications

- Conditions
  - For the input, the AC power supply source (V_{IN}) must range from $85V_{DC}$ to $230V_{DC}$. Monitor the input current so that it does not exceed the nominal rated current limit.
  - For the output, use an electronic variable load and/or a variable resistive load, which must be rated for at least $400V_{DC}$. Subsequently, vary the output load current up to the specified maximum limits. For detailed specifications of the system, refer to the provided datasheet.
- Setup

To determine the efficiency and consequently the total power loss in the system, the following circuit diagram in Figure 4 is provided to demonstrate the setup that was used in this specific test. Considering the diagram in left-to-right order, AC power is supplied from the grid and passed through an isolation transformer electrically separating the equipment under test from an AC mains supply. An additional variable autotransformer is also utilized for the purpose of fine line voltage adjustment. To obtain accurate both single-phase AC input and DC output electrical power measurements, two digital power meters are connected to the appropriate DUT terminals. The adjustment of specific real power load is implemented with the combination of an electronic DC load (up to 400W) and a resistive load bank (up to 2.7kW).

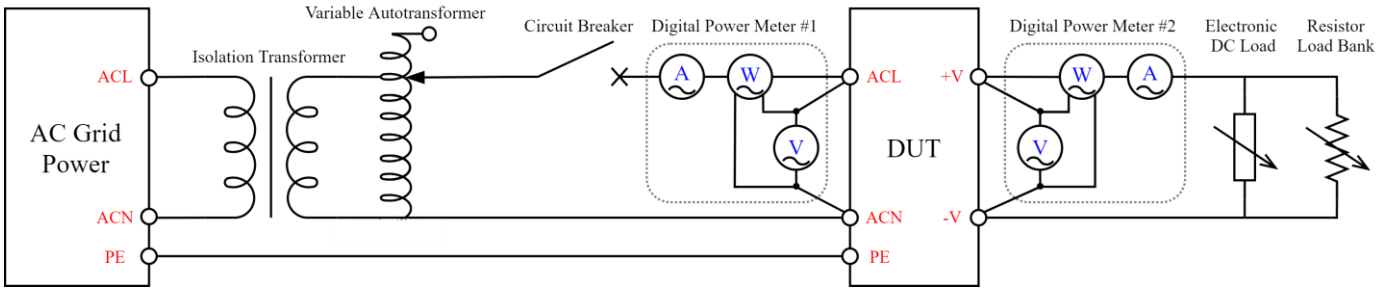


Figure 4: Test setup for a steady-state performance analysis

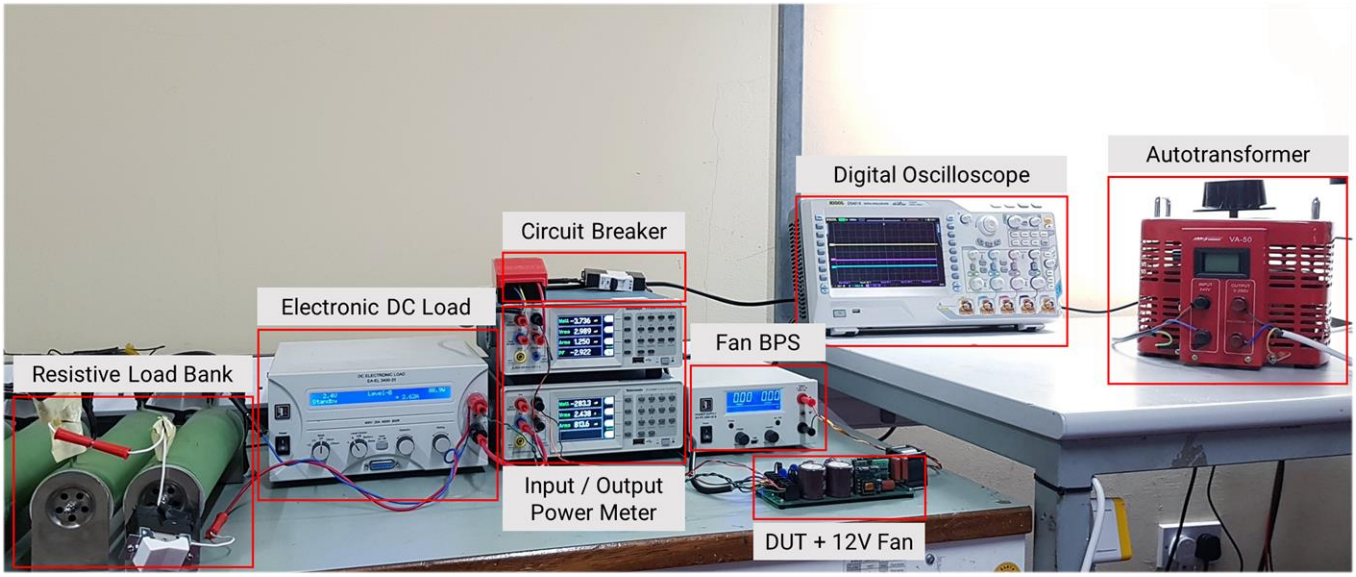


Figure 5: PFC evaluation board test arrangement

- Equipment

Table 3: List of the test equipment (steady-state operation)

No.	Equipment	Manufacturer	Model No.
1	Digital Multimeter	Brymen	BM869s
2	Power Quality Analyzer	Tektronix	PA1000
3	DC Electronic Load	EA Elektro-Automatik	EA-EL 3400-25
4	Digital Storage Oscilloscope	Rigol	DS4014
5	AC/DC Current Clamp Meter	Pico Technology	TA189
6	Differential Oscilloscope Probe	Pico Technology	TA043
7	Differential Oscilloscope Probe	Testec	TT-SI-51
8	Variable Autotransformer	Alde Tronics	VA-50
9	Isolation Transformer	Triad Magnetics	VPM240-20800
10	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ

- Procedure
  - Connect the input terminals (P, N, PE) of the evaluation board to the AC power source.
  - Connect the output terminals (DC+, DC-) to a positive and negative polarity connections of the electronic load and/or resistive load, respectively. “DC+” corresponds to a positive voltage of 400V_{DC} while “DC-“ corresponds to ground potential.
  - Ensure that the input voltage is within the specified limits and subsequently increase the output load from 0W to the required level without exceeding the maximal operating power limits.
  - Observe the start-up and steady state conditions for smooth switching waveforms to be sure that the system is operating correctly.

3.2 Efficiency, Power Factor and THD

The data provided below demonstrates universal 2kW (9A-Input) boost PFC converter efficiency with data points of a 100W output load step. Typical load efficiency is dependent on parameters such as the input voltage and the output load. Both are captured with high-line (230V_{RMS}), low-line (115V_{RMS}) and 85V_{RMS} input voltage. Note, that the efficiency data depicted in Figure 6 accounts for the losses in the EMI filter stage and the 12V bias supply. The fan power consumption is not included and is powered externally. Therefore, does not influence the total power loss of the system. The efficiency data was recorded only after thermal stability of the device under test was achieved.

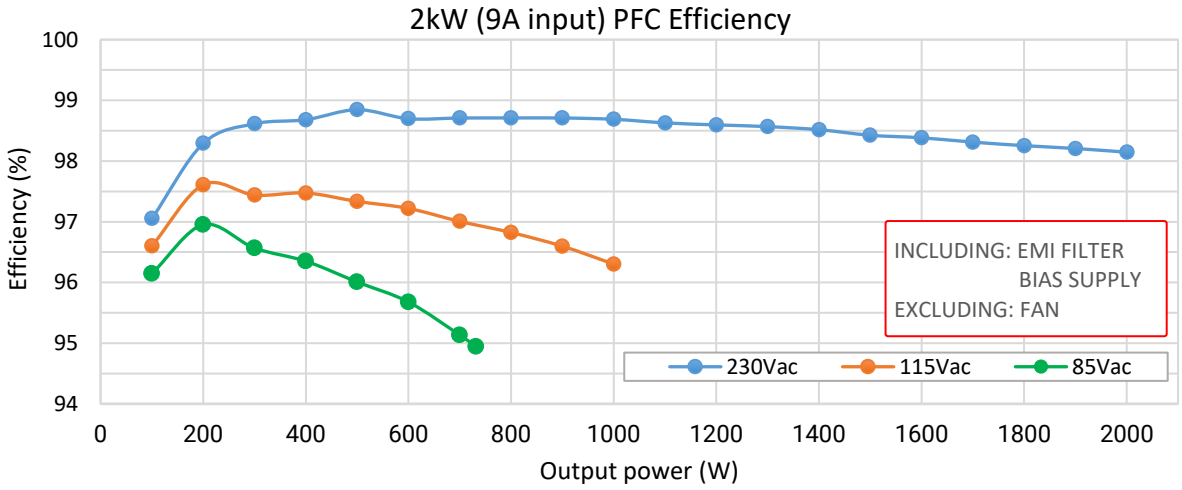


Figure 6: PFC stage efficiency for (V_{IN} = 230V_{AC}, 115V_{AC} and 85V_{AC}) with a load step of 100W

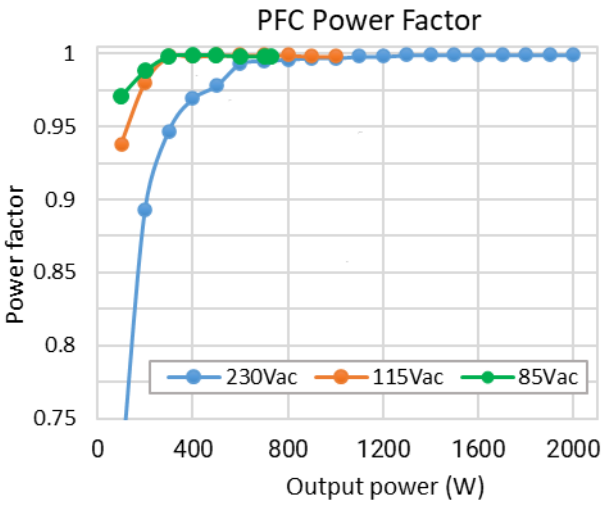


Figure 7: Power factor measurement with a load step of 100W

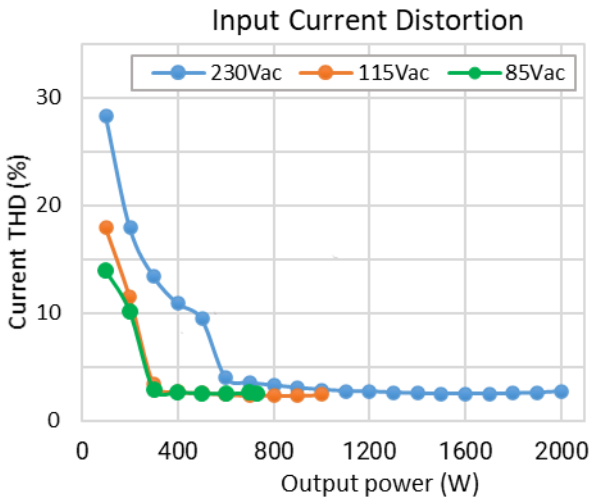


Figure 8: Input current distortion (ATHD) with a load step of 100W

Table 4 provides a more detailed breakdown of the efficiency measurements for an output load step of 200W for three different AC input voltage levels. For the instrument measurement accuracy, refer to the *Appendix* section.

Table 4: Measured efficiency of the universal 9A-Input PFC evaluation board

Input	Power Factor	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
$230V_{AC}$	0.893	230.73	0.9881	203.72	394.77	0.512	200.24	98.29
	0.969	229.92	1.8199	405.36	395.04	1.0167	400.01	98.68
	0.993	229.8	2.6631	608.01	395.02	1.5262	600.09	98.70
	0.996	229.9	3.5381	810.58	395.22	2.0308	800.12	98.71
	0.997	230.56	4.4071	1013.6	395.43	2.5312	1000.3	98.69
	0.998	230.43	5.2922	1217.4	395.62	3.0423	1200.3	98.60
	0.999	229.88	6.1745	1421.7	395.87	3.5419	1400.6	98.52
	0.999	230.32	7.0703	1626.5	396.02	4.0533	1600.2	98.38
	0.999	229.57	7.9899	1932.2	396.33	4.55	1800.2	98.25
	0.999	230.17	8.8666	2038.4	396.73	5.0451	2000.6	98.15
$115V_{AC}$	0.98	115.11	1.8156	204.92	394.48	0.5194	200.02	97.61
	0.998	115.74	3.5521	410.45	394.45	1.0268	400.08	97.47
	0.999	115.51	5.3497	617.18	394.62	1.5592	600.02	97.22
	0.999	115.13	7.1869	826.28	394.84	2.0561	800.03	96.82
	0.998	115.29	9.025	1038.6	395.12	2.5389	1000.3	96.30
$85V_{AC}$	0.988	85.57	2.4406	206.3	394.43	0.5266	200.01	96.95
	0.999	85.02	4.8911	415.3	394.4	1.0345	400.14	96.35
	0.998	85.61	7.3375	627.15	394.54	1.5759	600.05	95.68
	0.998	85.73	8.9739	770.97	394.71	1.8753	732.01	94.95

3.3 No load and light load operation

To reduce a power loss in the system, the narrowing of the PFC operating angle is deployed (Figure 9). It is present for either of the half-line cycles below the output power of 65W. This ensures that the system can comply with the power factor requirements even at light loads.

For extreme light load or no-load, low THD is usually not a requirement which allows the PFC to operate in a burst-mode (Figure 10). It is achieved by effectively turning off the PFC for a brief period (on the order of milliseconds) until the output voltage sags enough to re-enable the power supply drive. Due to this periodic disabling of the main power drive circuitry at very-low-load or no-load conditions, the total power consumption of the system is much less.

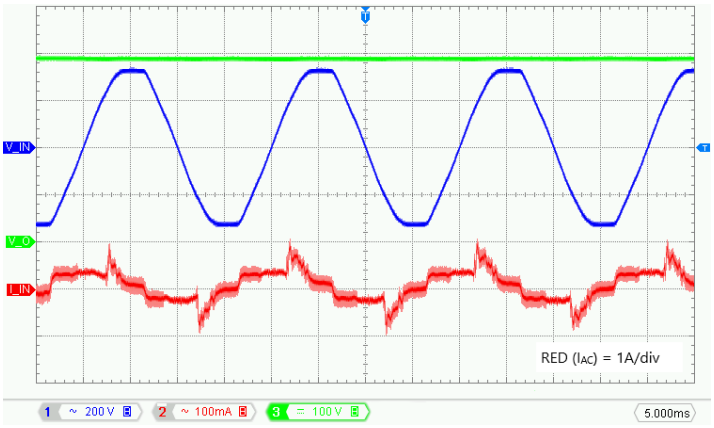


Figure 9: Reduced conduction angle operation (P_{OUT} = 50W)

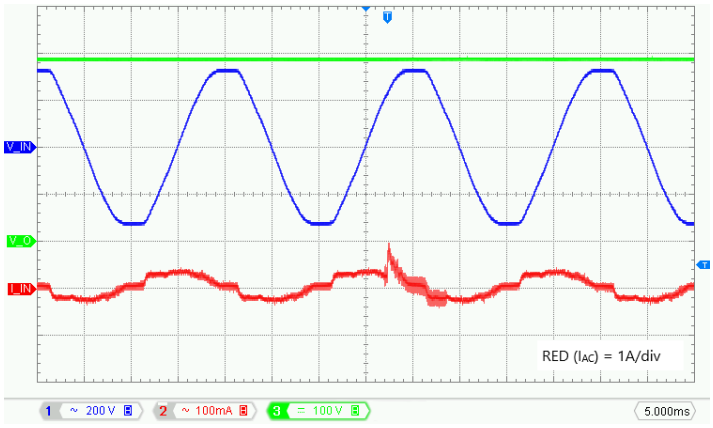


Figure 10: Burst-mode operation (P_{OUT} = 0W)

3.4 Digital Multi-mode operation

Reducing the switching frequency at light loads minimizes both the switching losses and gate-driving losses thereby improves the overall efficiency of the PFC system. Digital multi-mode technique is controlled based on the input current measurements and can be realized as follows:

- (33kHz for $I_{IN(AC)} \leq 2.5A_{RMS}$)
- (66kHz for $I_{IN(AC)} \geq 2.5A_{RMS}$)

In addition, boosted efficiency at light loads ($P_{IN} \leq 550W$) has negligible impact on electromagnetic interference (EMI) noise. Figure 11 below demonstrates waveforms of interest for 33kHz as well as the 66kHz operation in Figure 12.

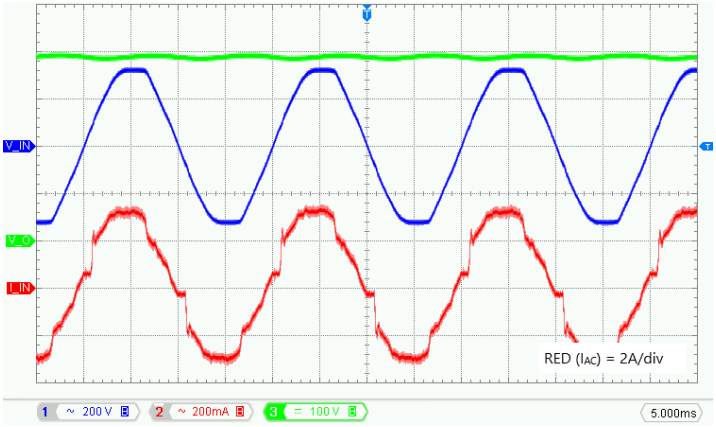


Figure 11: Switching frequency of 33kHz at V_{IN} = 230V_{RMS}, P_{IN} = 500W

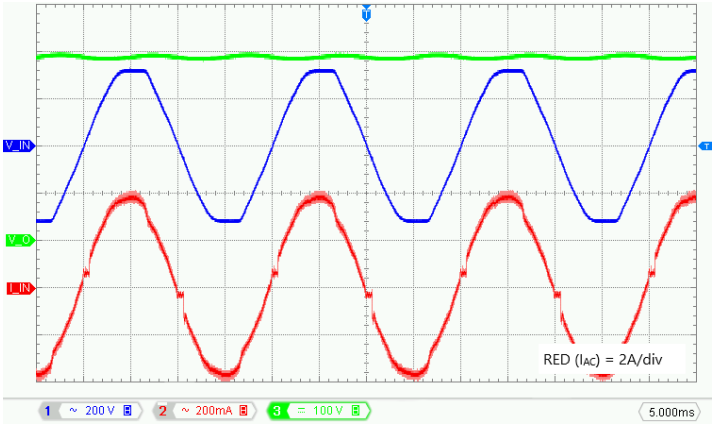


Figure 12: Switching frequency of 66kHz at V_{IN} = 230V_{RMS}, P_{IN} = 600W

3.5 Steady-state waveforms

The steady-state waveforms of the PFC board for both low-line (Figure 13) and high-line (Figure 14) are provided below. Each of the different line voltage levels demonstrate the PFC converter operating with 100% of a full load.

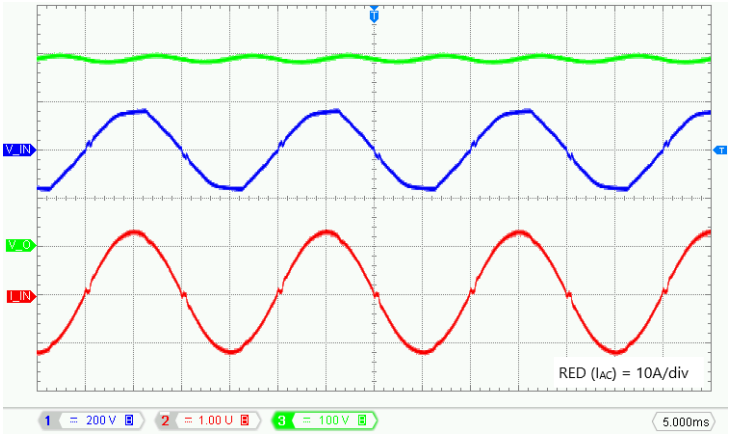


Figure 13: Steady state waveforms at V_{IN} = 115V_{RMS} and 1000W load

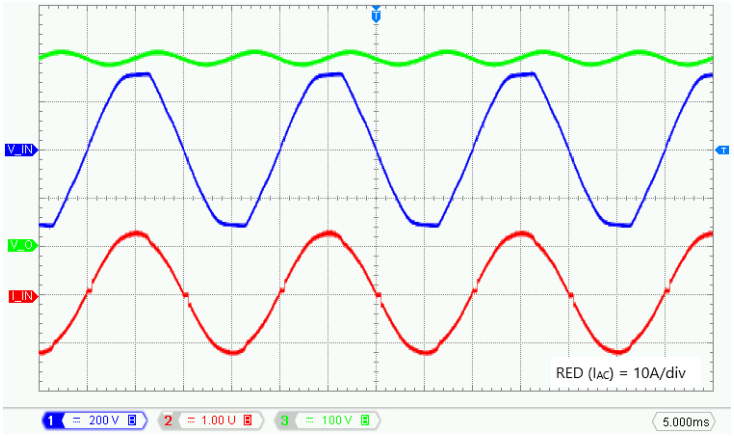


Figure 14: Steady state waveforms at V_{IN} = 230V_{RMS} and 2000W load

Waveforms in Figure 15 and Figure 16 highlight both the output voltage and the flying capacitor voltage ripple, respectively.

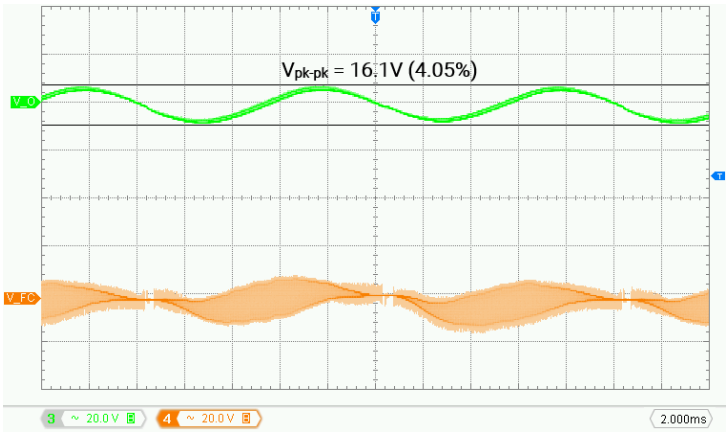


Figure 15: Output (C_{Bulk}) and flying capacitor (C_2) voltage ripple at V_{IN} = 115V_{RMS} and 1000W output load

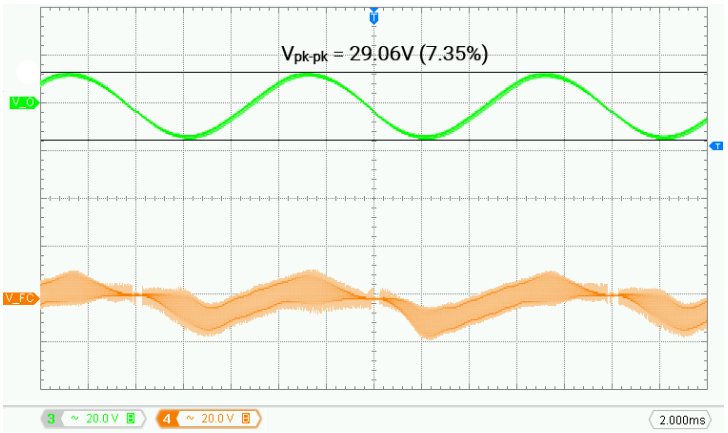


Figure 16: Output (C_{Bulk}) and flying capacitor (C_2) voltage ripple at V_{IN} = 230V_{RMS} and 2000W output load

Switch node waveforms for a positive half line cycle with duty ratio (D > 0.5) in Figure 17 and (D < 0.5) in Figure 18 are demonstrated below.

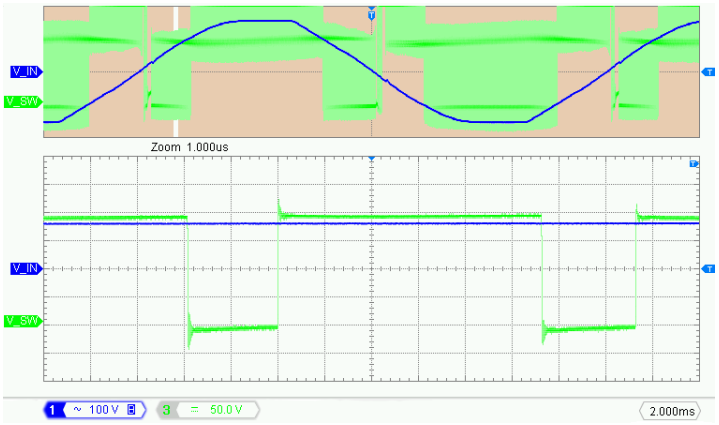


Figure 17: Switch node waveform with D > 0.5, V_{IN} = 230V_{AC}, P_{OUT} = 2000W

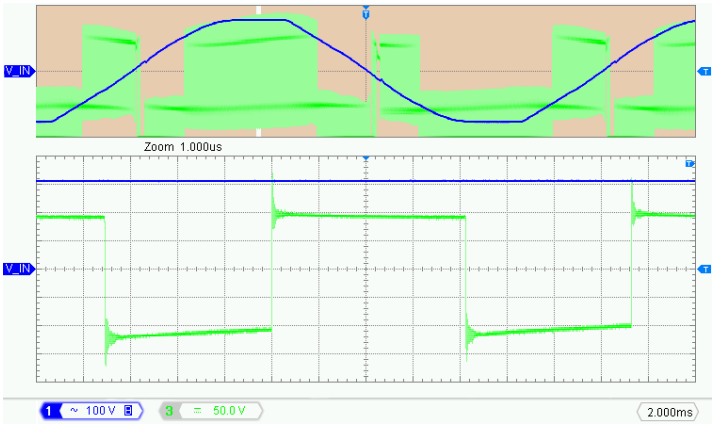


Figure 18: Switch node waveform with D < 0.5, V_{IN} = 230V_{AC}, P_{OUT} = 2000W

4. Start-up and inrush current

Both low-line ($115V_{AC}$) and high-line ($230V_{AC}$) start-up sequence waveforms with the focus on inrush current of the PFC converter are demonstrated in Figure 19 and 20, respectively. The inrush current is handled by a 7.5A rated 10Ω NTC thermistor which is subsequently bypassed with a relay during a steady state operation.

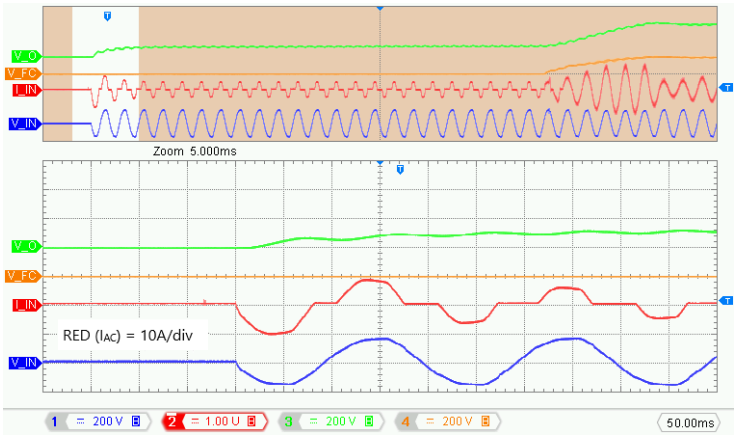


Figure 19: Switch on phase angle of $115V_{AC}$ input voltage (Φ = 0°) at 680W output load

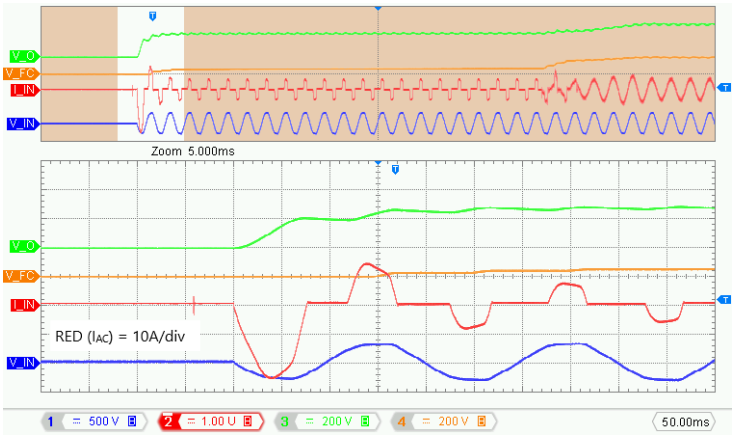


Figure 20: Switch on phase angle of $230V_{AC}$ input voltage (Φ = 0°) at 1000W output load

Due to implemented state machine in the PFC stage, a certain amount of time is required for the start-up of the converter once the input and the output voltages are detected given that they are within predefined safe operating limits. Figure 21 and 22 highlight the boost subsequence of the start-up procedure which brings the output voltage to the nominal voltage of $400V_{DC}$.

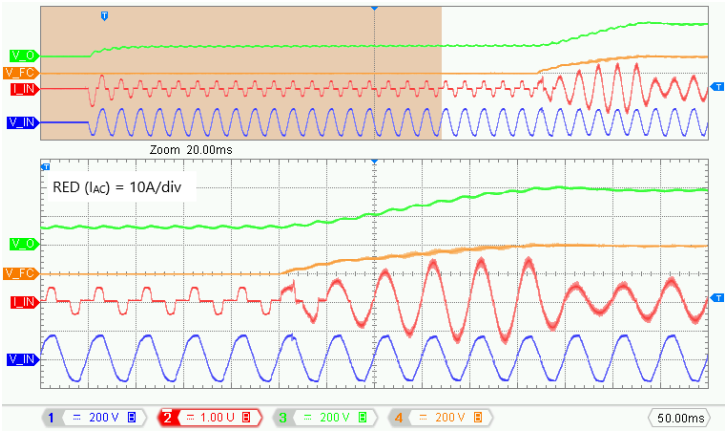


Figure 21: Boost subsequence of the start-up at $115V_{AC}$ and 680W output load

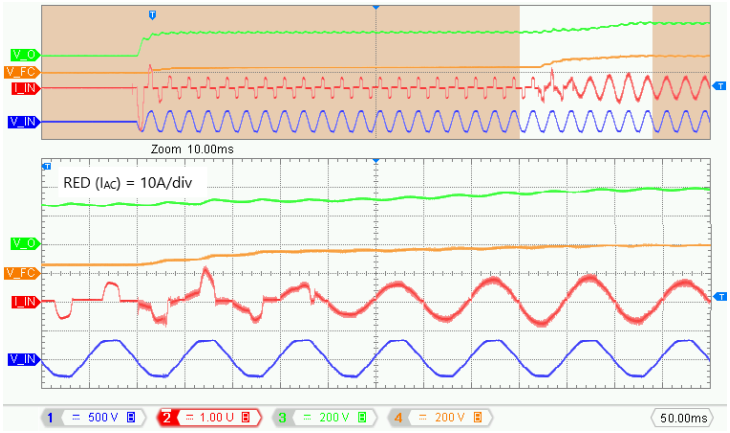


Figure 22: Boost subsequence of the start-up at $230V_{AC}$ and 1000W output load

5. Voltage balance

The 3-level bridgeless totem-pole PFC utilizes series-connected 150V MOSFET switching devices. To increase the reliability and to prevent the voltage distribution imbalance between those devices, the additional circuitry is required. The combination of actively controlled 5.4µF film capacitor C_2 and two passively controlled 47nF ceramic capacitors C_1 and C_3 as well as the additional 6 x 100V TVS devices are used to assist the HF switching leg as shown in Figure 23.

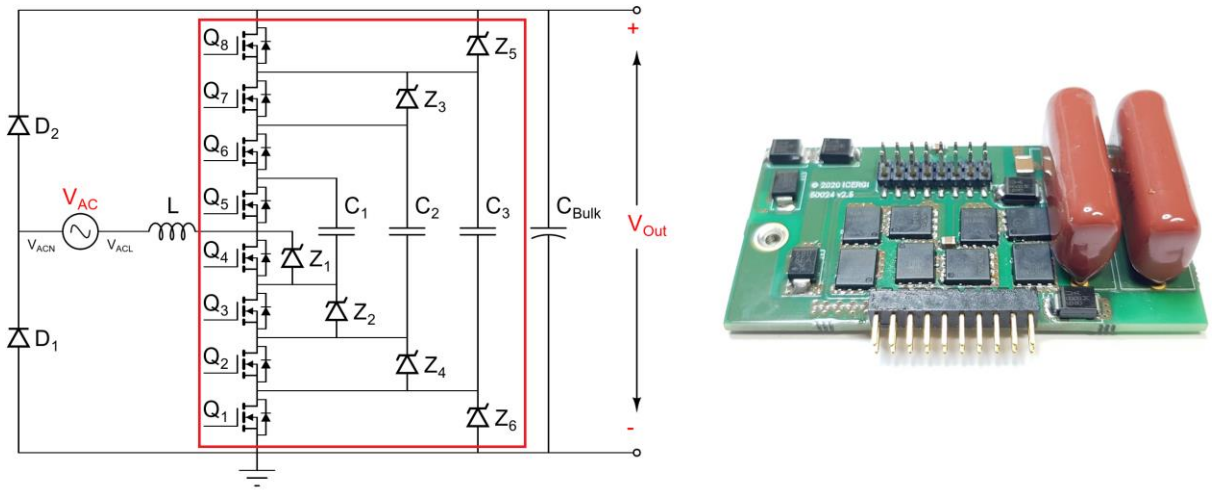


Figure 23: Voltage balance enforcement of a HF switching leg highlighted in red (left) and ICERGi PFC power card (right)

The following waveforms in Figure 24 and 25 demonstrate all three-flying capacitor (C_1, C_2, C_3,) voltage levels as well as the output voltage (C_{Bulk}) for both positive and negative half line cycles. It is evident that during both low-line and high-line cases voltage levels of the flying capacitors are well within 150V limit at any given time instant. Note that the each of the oscilloscope channels have the bandwidth limit of 20MHz enabled for the purpose of clearer results.

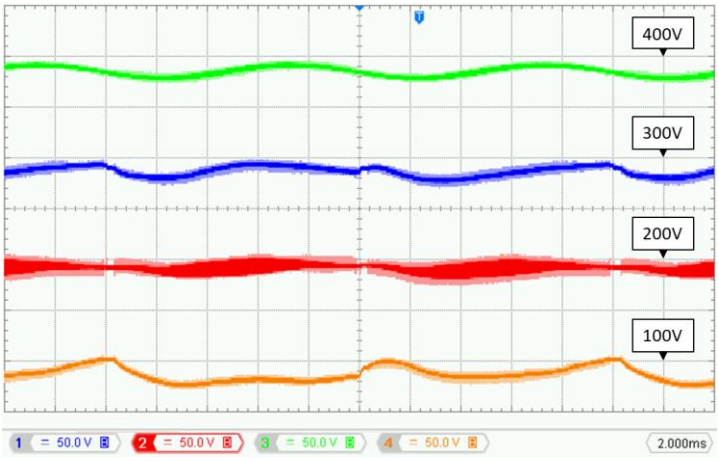


Figure 24: Operational waveforms at V_{IN} = 115V_{AC} and P_{OUT} = 1000W
(C_{Bulk} = GREEN, C_3 = BLUE, C_2 = RED, C_1 = ORANGE)

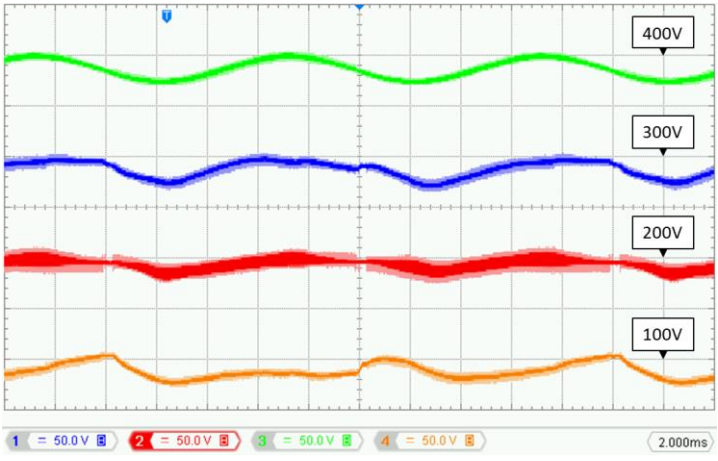


Figure 25: Operational waveforms at V_{IN} = 230V_{AC} and P_{OUT} = 2000W
(C_{Bulk} = GREEN, C_3 = BLUE, C_2 = RED, C_1 = ORANGE)

6. Dynamic load response

This section provides results regarding the load transient performance of the 9A universal input PFC as well as the evaluation method used to conduct such a test. Results are captured for both high-line and low-line voltages with step load changes from 0% - 50%, 50% - 100% and 0% - 65%, 35% - 100% of the maximum load, respectively.

6.1 Test specifications

- Conditions
  - Input voltage and output load must be adjusted correctly to obtain similar transient response results. It is recommended to test the PFC system at full load for low-line ($115V_{AC}$) and high-line ($230V_{AC}$) before subjecting the system to sudden load fluctuations.
  - The negative side of the output capacitor must be used as a single point ground for all measurement connections. The oscilloscope used to read the output waveform must be connected directly across C_{Bulk}.
  - If a resistive load bank is employed, a use of lower inductance resistors is suggested.
  - Both the resistive load bank and DC electronic load are controlled with switches 1 and 2. However, the resistive load is turned on and off with a mechanical SPST switch. Thus, a slew rate for a rising/falling edge of the output current transition cannot be controlled.
- Setup

The circuit diagram provided in the Figure 26 below demonstrates the test setup used to carry out relevant step load results. The order of both the electronic DC load and the resistor load bank are interchanged in order to achieve the required level of step load.

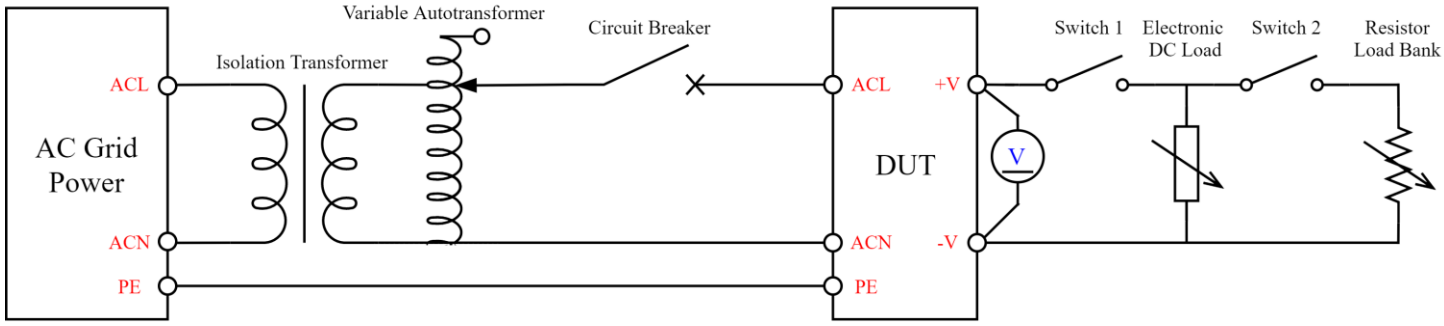


Figure 26: Circuit diagram of a test setup (dynamic load response)

- Equipment

Table 5: List of the test equipment (load transient response)

No.	Equipment	Manufacturer	Model No.
1	DC Electronic Load	EA Elektro-Automatik	EA-EL 3400-25
2	Digital Storage Oscilloscope	Rigol	DS4014
3	AC/DC Current Clamp Meter	Pico Technology	TA189
4	Differential Oscilloscope Probe	Pico Technology	TA043
5	Differential Oscilloscope Probe	Testec	TT-SI-51
6	Variable Autotransformer	Alde Tronics	VA-50
7	Isolation Transformer	Triad Magnetics	VPM240-20800
8	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ

- Procedure
  - Connect the input terminals (P, N, PE) of the evaluation board to the AC power source. Ensure that the input voltage is adjusted to satisfy the specified absolute maximum limits before start-up and during/after load transients.
  - Connect the output terminals (DC+, DC-) to a positive and negative polarity connections of the electronic load and/or resistive load, respectively. "DC+" corresponds to a positive voltage of $400V_{DC}$ while "DC-" corresponds to ground potential.
  - Supply power to the PFC and increase the output load to the necessary transient response load level. Ensure that the input voltage is adjusted if needed, to prevent excess amount of input current during 100% output load operation.
  - Once the operation of the PFC is confirmed at different output load levels, proceed to the actual step load test.
  - Observe sudden load transients by measuring the output voltage and the output current waveforms for validation of the systems capability to regulate the output voltage.

6.2 Results

This section captures waveforms of interest to demonstrate the settling characteristics after the load transient occurs. Transient response waveforms include input current I_{IN} (RED), output current I_{OUT} (BLUE), flying capacitor voltage $V_{FC(200V)}$ (ORANGE) and the output voltage V_O (GREEN). Figure 27 and 28 demonstrates the output voltage transient response for low-line (0% - 65% output load) and high-line (0% - 50% output load) respectively.

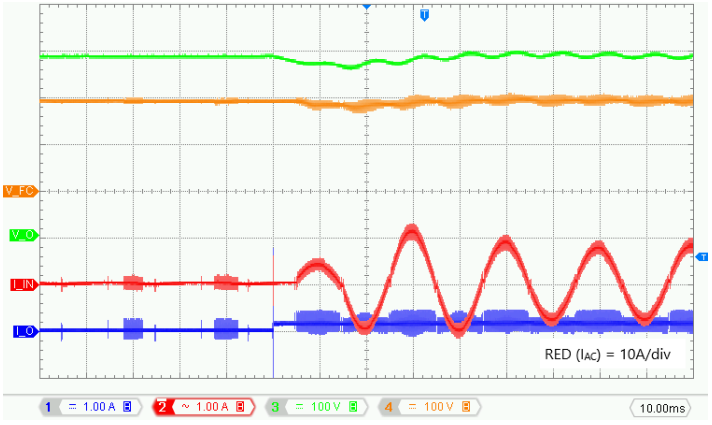


Figure 27: 0W to 680W step load at line voltage of V_{IN} = $115V_{AC}$

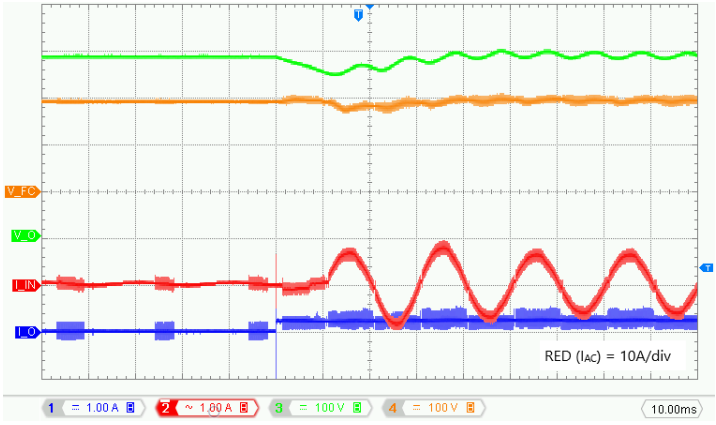


Figure 28: 0W to 1000W step load at line voltage of V_{IN} = $230V_{AC}$

Figure 29 and 30 depicts the output voltage regulation and the time it takes for the voltage to recover for low-line (35% – 100%) and high-line (50% - 100%).

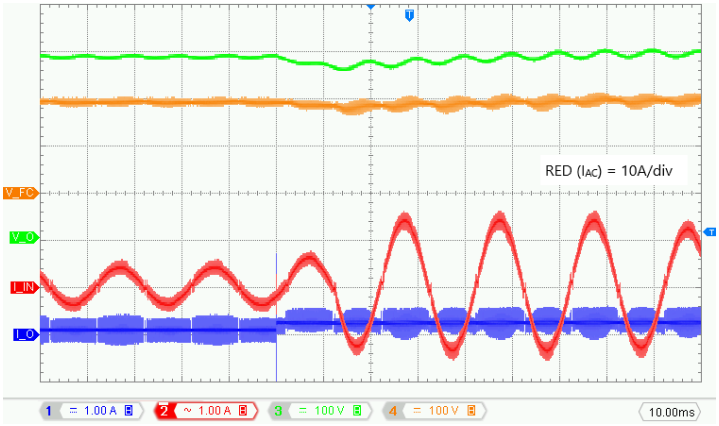


Figure 29: 340W to 1000W step load at line voltage of V_{IN} = $115V_{AC}$

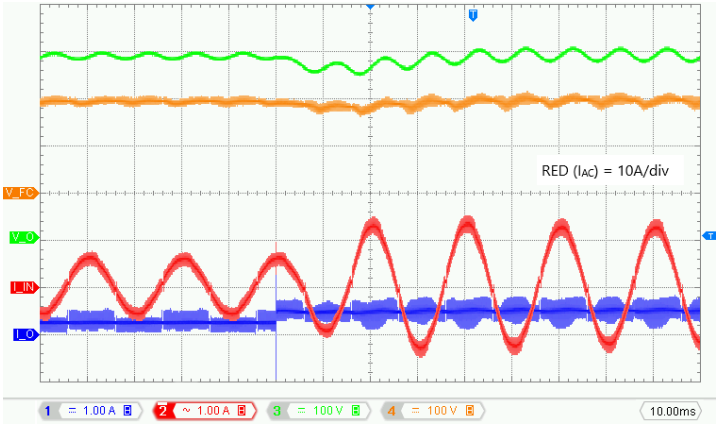


Figure 30: 1000W to 2000W step load at line voltage of V_{IN} = $230V_{AC}$

7. AC frequency transient

This section includes the test results of the PFC evaluation board subjected to varying input voltage frequencies to test it against different worldwide power conditions. For this purpose, a programable AC source is used. However, due to limitations in the power handling of the test equipment, AC input voltage transients are only tested at low power. Input voltage frequency lockout and over/under frequency protection levels are fully adjustable in software. It takes several half-line cycles for the controller to detect and adjust the frequency level in the system. This is an intended behaviour based on the averaging method in order to prevent false frequency detection during other events such as surge, etc.

7.1 Test specifications

- Conditions
  - AC input frequency should be varied for a specified minimal and maximal frequency range (35Hz < f_{AC} > 75Hz). Both AC input frequency hard limits and under/over frequency lockout levels are specified in a separately provided datasheet document.
  - Given that the input AC frequency is varied enough so that UFLO (f_{AC} = 45Hz) or OFLO (f_{AC} = 65Hz) are detected – the PFC controller will maintain the normal operation only for a specified amount of switching cycles before turning itself off.
- Setup

The following circuit diagram in Figure 31 below demonstrates the test setup for validating the PFC systems ability to operate with different AC source frequencies.

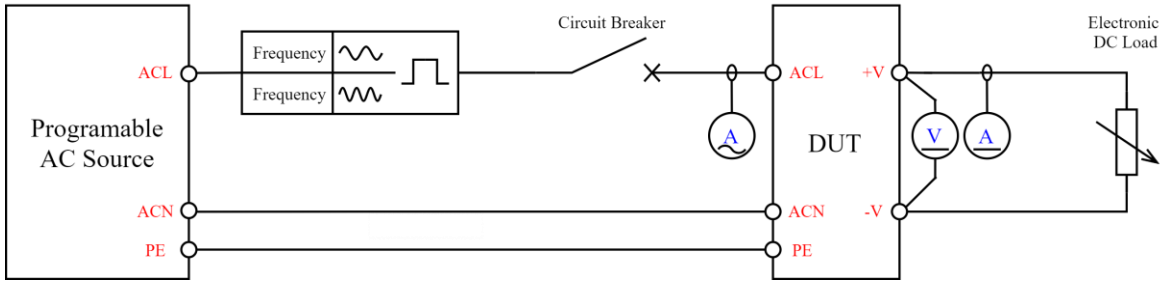


Figure 31: Circuit diagram of an AC input frequency transient test

- Equipment

Table 6 presents the list of the recommended test equipment.

Table 6: Test equipment (AC frequency transient)

No.	Equipment	Manufacturer	Model No.
1	DC Electronic Load	EA Elektro-Automatik	EA-EL 3400-25
2	Digital Storage Oscilloscope	Rigol	DS4014
3	AC/DC Current Clamp Meter	Pico Technology	TA189
4	Differential Oscilloscope Probe	Pico Technology	TA043
5	Differential Oscilloscope Probe	Testec	TT-SI-51
6	Programmable AC Source	Keysight	AC6801A

- Procedure
  - Connect the input terminals (P, N, PE) of the evaluation board to the programable AC power source. Ensure that the input voltage is adjusted to satisfy the specified absolute maximum limits before start-up and during/after frequency transients.
  - Connect the output terminals (DC+, DC-) to a positive and negative polarity connections of the electronic load and/or resistive load, respectively. "DC+" corresponds to a positive voltage of $400V_{DC}$ while "DC-" corresponds to ground potential.
  - Before supplying power to PFC, ensure that the AC input frequency is adjusted within the nominal frequency range.
  - Once the PFC is started and is operating in steady state for a given output load, adjust the input frequency slowly to confirm the appropriate functioning of the system.
  - Proceed to an AC input frequency transient test and observe operating conditions for a validation of the systems capability to respond to sudden changes in line frequency.

7.2 Results

The following test results cover PFC response results to different types of AC line frequency variation. Transient performance waveforms are provided for a frequency step up (Figure 32) as well as the step down (Figure 33). Furthermore, over frequency protection (OFP) is also verified which is depicted in Figure 34. However, due to the limitations in a frequency range of the test hardware, under frequency protection (UFP) could not be verified.

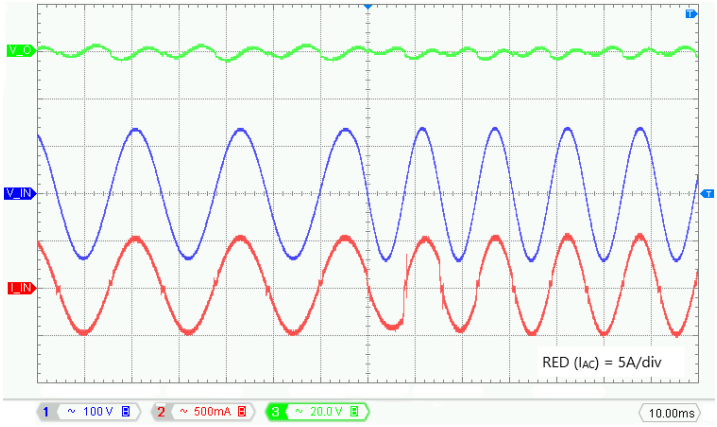


Figure 32: AC frequency variation 45 – 65Hz (V_{IN} = 95V_{AC}, P_{OUT} = 340W)

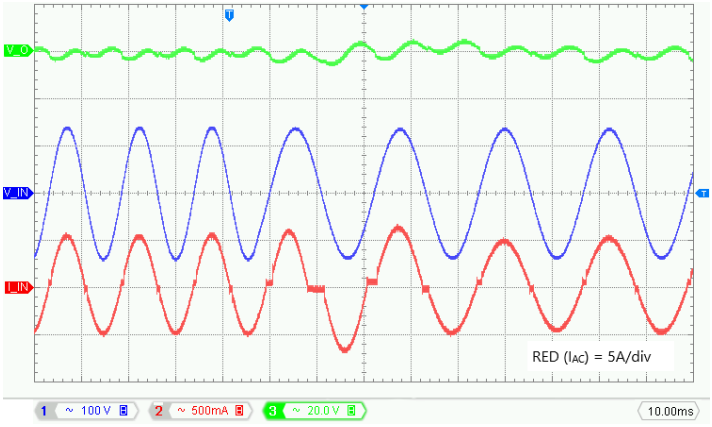


Figure 33: Frequency variation 65 – 45Hz (V_{IN} = 95V_{AC}, P_{OUT} = 340W)

Figure 34: Over frequency protection 50 – 80Hz (V_{IN} = 95V_{AC}, P_{OUT} = 340W)

8. Electromagnetic emissions (EMC)

8.1 Standards

Emissions were assessed to the following standards as per Table 7 below:

Table 7: Summary of EMC standards

Basic standard	Description	Performance criteria	Result
EN 55022/32	Conducted emissions	Class B	PASS
EN 55022/32	Radiated emissions	N/A	N/A
IEC 61000-3-2	Harmonic current emissions	Class A	PASS
IEC 61000-3-3	Voltage fluctuation and flicker	N/A	N/A

- Equipment

Table 8 presents the list of the recommended test equipment for both conducted and harmonic current emissions.

Table 8: List of the recommended equipment for EMC measurement

No.	Equipment	Manufacturer	Model No.
1	Power Quality Analyzer	Tektronix	PA1000
2	Spectrum Analyzer	Rigol	DSA815
3	Line Impedance Stabilization Network	Rohde & Schwarz	HM6050-2
4	Variable Autotransformer	Alde Tronics	VA-50
5	Isolation Transformer	Triad Magnetics	VPM240-20800
6	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ

8.2 Conducted emission (EN 55022/32)

- Conditions
  - For conducted emissions the principal requirement is the placement of the EUT with respect to ground plane and the line impedance stabilization network (LISN) as well as disposition of the mains cable and earth connection(s). Even though it is not demonstrated in the Figure 35 below, there is a stray capacitance between the DUT and the ground reference plane (GRP) which is an important part of the coupling path.
  - Pre-compliance test regarding the conducted emissions was carried out with recommended table-top of the DUT to other conducting surface suggested clearances in mind. In particular, the required separation distance of the DUT from both vertical and horizontal ground planes are 400 mm and 800 mm, respectively.
  - Note, that due to the high stray capacitance coupling from resistor load bank to GRP, the output of the PFC evaluation board is fitted with an additional common mode choke to minimize the measurement error.
- Setup

The receiver bandwidth is set to 9 kHz with a sweep duration of 10s. Note that the results are displayed in a logarithmic scale with a range of frequencies from 150 kHz to 30 MHz. The important parameters of this test are summarized in the Table 9 below.

Figure 35 demonstrates the recommended example of a conducted emissions test setup.

Table 9: Device parameters for conducted emissions

Device name	Parameter	Value
Spectrum Analyzer	Frequency range	150 kHz – 30 MHz
	Sweep time	5/10s
	Filter type	EMI
	Resolution Bandwidth	9 kHz
	Frequency scale	Logarithmic
LISN	Conductive phase	Live
DUT	Input voltage	$230V_{RMS}$
	Output power	2000W
	Output CM choke	90µH

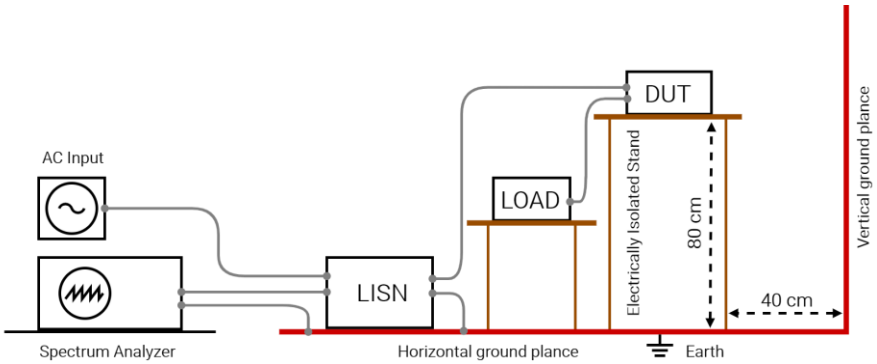


Figure 35: Conducted emissions test setup

- Procedure
  - Connect the spectrum analyser to the limiter, LISN and DUT. Ensure that the cable between the DUT and LISN is as short as possible to prevent power cord acting as an antenna.
  - Select the frequency bandwidth for conducted emissions test as per CISPR requirements of (150 kHz – 30 MHz).
  - Setup the appropriate limit lines and correction factors based on the detection type (quasi-peak, average).
  - Switch on the DUT and adjust the output load to a required level.
  - Measure conducted emissions with quasi-peak and average detection modes to obtain results.
- Results

In both Figure 36 (average) and Figure 37 (peak) conducted EMI measurements are provided with the corresponding class B limits. It is evident that the DUT complies with the standard while offering at least 20dBµV margin across most of the frequency range of interest.

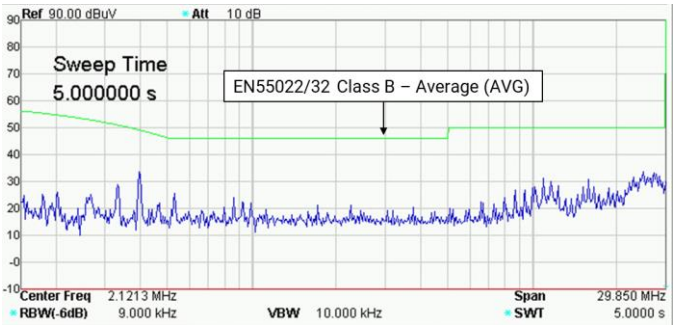


Figure 36: Conducted emissions with average detector

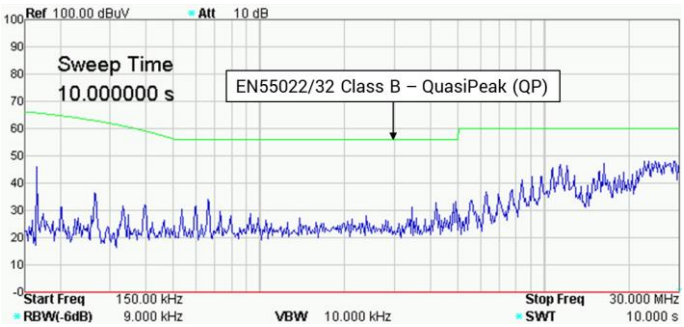


Figure 37: Conducted emissions with peak detector

8.3 Harmonic current emissions (IEC 61000-3-2)

- Conditions
  - For input current harmonics measurement, all (even and odd) harmonics up to 50th are considered.
  - The supplied crest factor V_{cf} on average is measured to be 1.3873. It falls outside of the required range of $1.4 \leq V_{cf} \geq 1.42$.
- Setup

Figure 38 indicates the basic measurement technique for mains harmonic emissions.

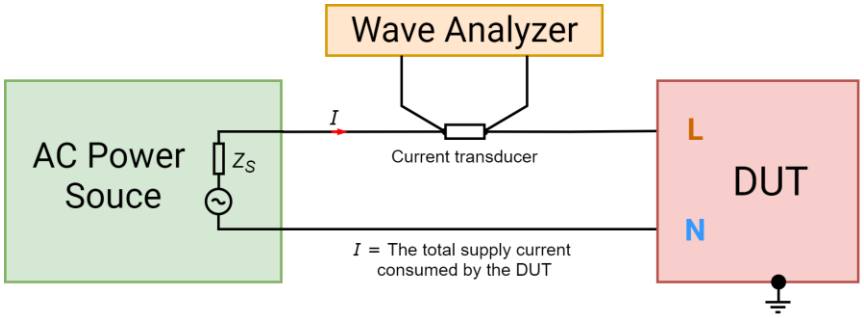


Figure 38: Harmonic current emissions measurement circuit

- Procedure
  - Configure the power analyser for AC power line harmonics according to IEC 61000-3-2 standard (sequence, range, acquisition format, etc.)
  - Power up the DUT and adjust both the input voltage and the output load.
  - Once the PFC system is in steady state and it is configured for a given set of operating conditions, initiate the test.
  - Monitor the steady state conditions for smooth switching waveforms to be sure that the system is operating correctly until the test is completed.
  - Repeat the test for a different input line voltage.
- Results

This section provides test results of the harmonic analysis for IEC/EN 61000-3-2 pre-compliance to the 50th order. Current harmonics and the appropriate test summary are provided only for high line ($230V_{RMS}$) in the Table 10 below. Note that a full breakdown of all harmonics is not provided and can only be found in a separately generated report including the test results for low line.

Table 10: Test summary of IEC 61000-3-2 at V_{IN} = $230V_{AC}$, P_{IN} = 2000W

Test Summary		General Results			
Test type	IEC 61000-3-2	Test value	Average	Minimum	Maximum
Test date / time	1/18/2021 1:31 PM	Watts (kW)	1.9859	1.9818	1.9893
Overall test status	PASS	Power Factor (m)	998.86	998.74	998.92
Pre-comp category	Class A	Amps fundamental (A)	8.6723	8.6564	8.6959
Specified voltage	$230V_{AC}$	V_{RMS} (V)	229.16	228.53	229.74
Specified frequency	50 Hz	Frequency (Hz)	49.856	49.839	49.869
Test duration	00:02:30	A_{RMS} (A)	8.6759	8.6507	8.7066
Ambient temperature	23°C ± 3°C	Vcf	1.3873	1.3845	1.3921
Humidity	< 75%				

9. EMC immunity

EN 61000-6-1 is a part of IEC 61000 for EMC immunity requirements that applies to electrical and electronic equipment intended for use in residential, commercial, public and light-industrial locations.

9.1 Standards

Emissions were assessed to the following standards as per Table 11 below.

Table 11: Summary of EMC immunity standards

Basic standard	Description	Performance criteria	Result
EN 61000-4-2	Electrostatic discharge	N/A	N/A
EN 61000-4-3	Radiated emissions	N/A	N/A
EN 61000-4-4	Electrical fast transients	Class A	PASS
EN 61000-4-5	Input voltage surge	Class A	PASS
EN 61000-4-6	Conducted disturbances	N/A	N/A
EN 61000-4-8	Power frequency magnetic field	N/A	N/A
EN 61000-4-11	Voltage dips, variations and short interruptions	Class A / B	PASS

9.2 Input voltage surge (EN 61000-4-5)

- Conditions

Table 12: Surge test conditions and device parameters

Equipment	Description	Value
DUT	Output power	2000W
	Input voltage	$230V_{AC}$
Surge module	Repetition rate	15s
	Phase step	5°
	Pulse rise time	6.4µs ± 20%
	Pulse duration	16µs ± 20%
Other	Power lead length	1.5m

- Setup

The coupling generator UCS 500 has an integrated coupling network in accordance with IEC 61000-4-5 and is shown in Figure 39.

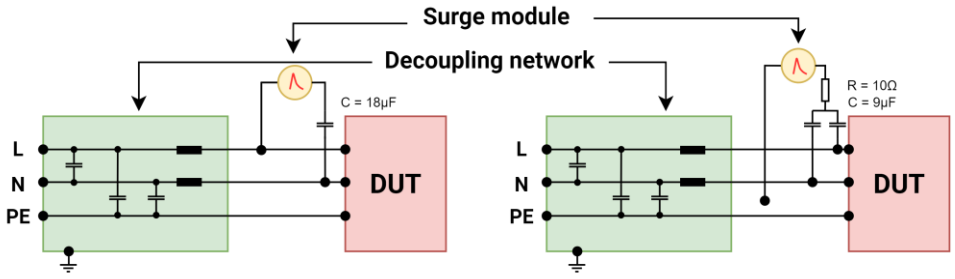


Figure 39: Input voltage surge test setup with line-to-line coupling (left) and line-to-earth (right)

- Equipment

Table 13: List of the input surge test equipment (61000-4-5)

No.	Equipment	Manufacturer	Model No.
1	Ultra-compact EM simulator	EM Test	UCS500-M4
2	Digital Storage Oscilloscope	Rigol	DS4014
3	AC/DC Current Clamp Meter	Pico Technology	TA189
4	Differential Oscilloscope Probe	Pico Technology	TA043
5	Differential Oscilloscope Probe	Testec	TT-SI-51
6	Isolation Transformer	Triad Magnetics	VPM240-20800
7	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ

- Procedure

Surge pulses were applied synchronized to the voltage phase at the respective angle and the peak value of the AC voltage wave for both positive and negative polarities. The surge test was applied to both line-to-line (differential mode) and line(s)-to-earth (common mode). The test voltage was increased by steps up to the test level specified in the tabulated standard results. For the iteration of the standard test procedure as per IEC 61000-4-5 refer to Figure 40 below. Test conditions and other important parameters are provided in the Table 12 above.

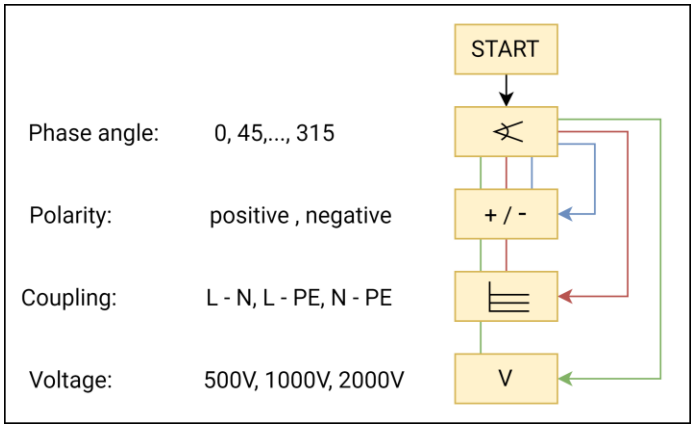


Figure 40: Input voltage surge iteration process

- Results

Table 14: Common and differential mode surge immunity test results (IEC 61000-4-5)

Basic standard	Surge mode	Level	Voltage (V)	Pre-comp Class	Pass / Fail
IEC 61000-4-5	Differential (L - N)	1	500	Class A	PASS
		2	1000		PASS
		3	2000		PASS
		4	4000	N/A	N/A
	Common (L/N - PE)	1	500	Class A	PASS
		2	1000		PASS
		3	2000		PASS
		4	4000		PASS

9.3 Voltage dips, variations and short interruptions (EN 61000-4-11)

PFC system is required to meet the relevant hold-up time (HUT) requirements to avoid abrupt shut-down and maintain the operation of equipment for a few line cycles. Likewise, it is required to regulate the output voltage during and after short-term reductions in a supply voltage.

- Setup

Figure 41 indicates the test setup for voltage dips and short interruptions.

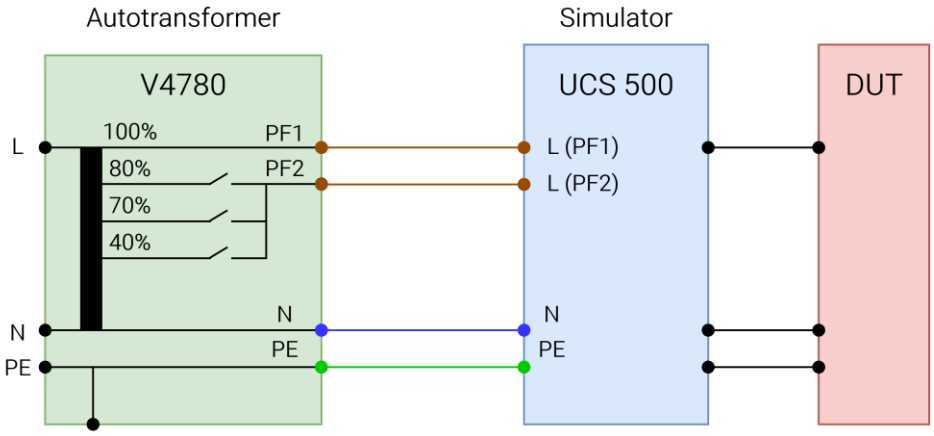


Figure 41: Voltage dips and short interrupts test setup

- Equipment

Table 15 presents the list of the recommended test equipment for volta variations, dips and short interrupts.

Table 15: List of the voltage dips test equipment (61000-4-11)

No.	Equipment	Manufacturer	Model No.
1	Ultra-compact EM simulator	EM Test	UCS500-M4
2	Digital Storage Oscilloscope	Rigol	DS4014
3	AC/DC Current Clamp Meter	Pico Technology	TA189
4	Differential Oscilloscope Probe	Pico Technology	TA043
5	Differential Oscilloscope Probe	Testec	TT-SI-51
6	Isolation Transformer	Triad Magnetics	VPM240-20800
7	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ
8	Tapped Auto Transformer	EM Test	V4780

- Procedure

Depending on the specified test parameters in Table 14, the test voltage is changed to a lower value or interrupted for a certain duration and a certain phase angle. Voltage variations are related to the nominal value of the supply voltage for both low-line ($115V_{AC}$) and high-line ($230V_{AC}$). Note that each voltage dip or dropout is repeated 3 times with 10 seconds between each. Table 16 summarizes the test conditions and corresponding results.

- Results

Table 16: Test results summary for voltage dips and interruptions

Voltage Dips							
Voltage (V_{AC})	**Voltage Dip (%)**	**Voltage Dip ($_{AC}$)**	**Duration (ms)**	**Phase Angle (°)**	**Power (W)**	**Pre-comp Class**	**Pass/Fail**
115	30	85	500	0 - 360	680	Class A	PASS
	60	46			680	Class B	PASS
230	30	161			1300	Class A	PASS
	60	92			680	Class A	PASS
Voltage Interruptions							
115	100	0	10	0 – 360	1000	Class A	PASS
230					2000	Class A	PASS
115			500	0	1000	Class B	PASS
230					2000	Class B	PASS

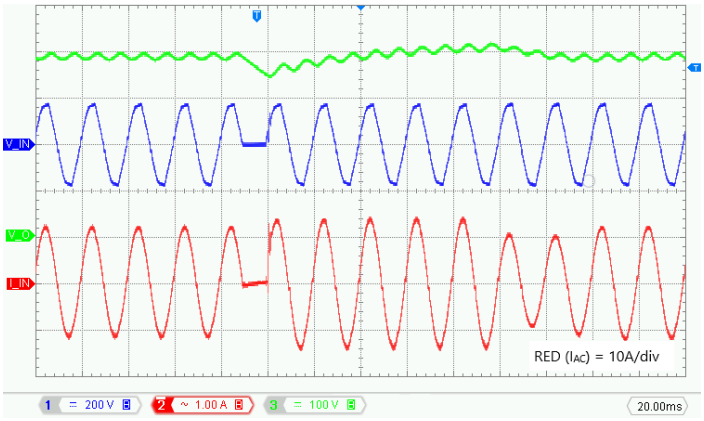


Figure 42: 10ms input voltage interrupt
(V_{IN} = 115V_{AC}, P_{OUT} = 1000W, V_{OUT} = 400V_{DC}, φ = 0°)

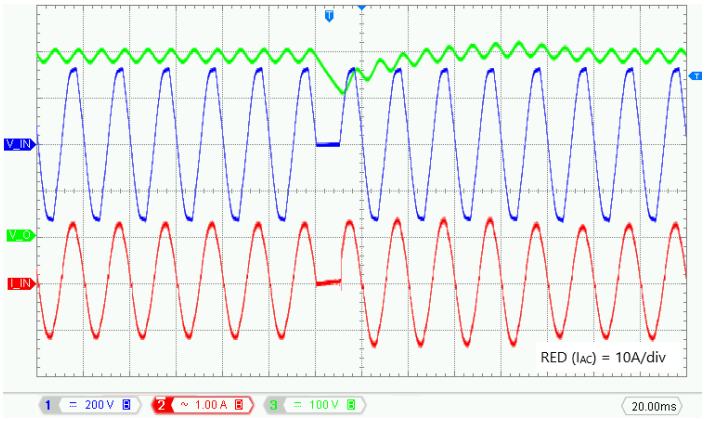


Figure 43: 10ms input voltage interrupt
(V_{IN} = 230V_{AC}, P_{OUT} = 2000W, V_{OUT} = 400V_{DC}, φ = 0°)

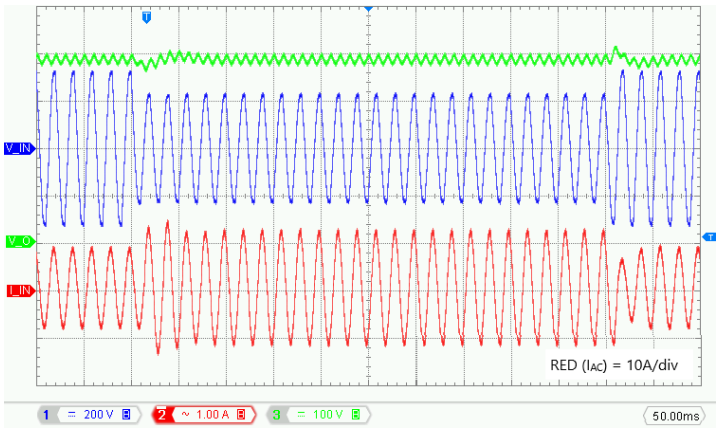


Figure 44: 30% (V_{AC} = 162) input voltage dip
(V_{IN} = 230V_{AC}, P_{OUT} = 1300W, V_{OUT} = 400V_{DC}, φ = 0°)

Figure 45: 60% (V_{AC} = 92) input voltage dip
(V_{IN} = 230V_{AC}, P_{OUT} = 680W, V_{OUT} = 400V_{DC}, φ = 0°)

10. Thermal measurements

To examine and better understand the thermal performance of the individual power components making up the PFC stage, maximum temperatures are captured and recorded.

10.1 Test specifications

- Conditions
  - It is achieved with a thermal imaging camera at the room temperature of 24.5°C with no enclosure for the device under test.
  - External fan operated at 12V was placed opposite to both input and output connectors to provide the forced air type of convection cooling.
  - This arrangement helps to transfer heat away from the most heat generating power devices with heatsinks (high-frequency MOSFETs, diode bridge rectifier) as well as the main inductor (Figure 46, 47).
  - Note that the board was operating with $220V_{AC}$ and 9A input current which was allowed to run for 15 minutes before any thermal images were captured.
- Setup

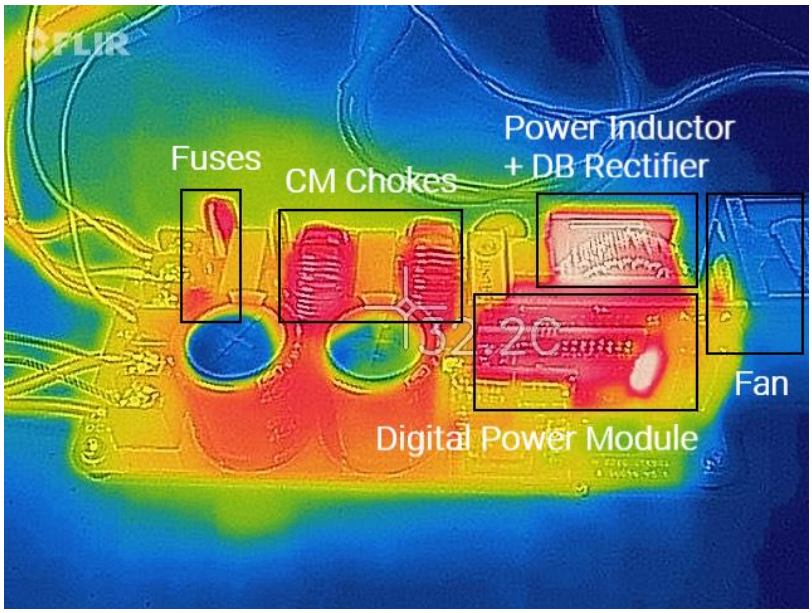


Figure 46: Horizontal thermal image of the PFC evaluation board + fan (right)

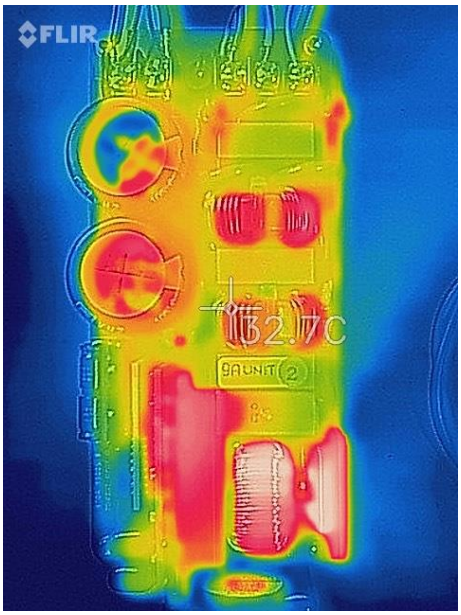


Figure 47: Vertical top-side thermal image

- Equipment

Table 17: List of the equipment (thermal measurement test)

No.	Equipment	Manufacturer	Model No.
1	DC Electronic Load	EA Elektro-Automatik	EA-EL 3400-25
2	Variable Autotransformer	Alde Tronics	VA-50
3	Isolation Transformer	Triad Magnetics	VPM240-20800
4	Tapped Auto Transformer	EM Test	V4780
5	Resistive Dump Load	CGS-TE Connectivity	TE1000B470RJ
6	Thermal Imaging Camera	FLIR One	435-0002-02-00
7	DC Fan	Sanyo Denki	SanAce 40

10.2 Results

Table 18 below shows the tabulated temperature results for the components of interest.

Table 18: Thermal performance results

Component	Description	Part number	Temperature (°C)
Input fuse	2 x 16A miniature fuse with pigtail	SPT5X20	35.5
Common-mode choke	2 x T38 ferrite cores (1.25mm wire)	B64290L0618X038	37.8
Diode bridge rectifier	1 x 8A 800V (single phase)	GBU8K	50.2
Main PFC inductor	1 x 500µH (0.9mm wire)	MS 106060-2	41.4
Power MOSFETs	8 x Vishay 150V MOSFETs	SQJ872EP	58.1

11. Revision history

Date	Version	Changes
16–02–2021	1.0	First release
18–02–2021	1.1	Document format changes, updated efficiency measurement data

12. Appendix

- Measurement accuracy
  - Power analyser (Tektronix PA1000)

Parameter	Specification
Voltage – V_{RMS}, V_{rmn}, V_{DC}	
V_{RMS} 45-850 Hz Accuracy	±0.05% of reading ±0.05% of range ±0.05 V
V_{RMS} 10 – 45Hz, 850 – 1MHz Accuracy	±0.1% of reading ±0.1% of range ± (0.02 * F)% of reading ±0.05 V
DC Accuracy	±0.1% of reading ±0.1% of range ± 0.05 V
Voltage – V_{pk+}, V_{pk-}	
Peak Accuracy	±0.5% of reading ± 0.5% of range + (0.02 * F)% of reading ±0.5 V
Current – A_{RMS}, A_{DC}	
A_{RMS} 45 – 850Hz Accuracy	±0.05% of reading ±0.05% of range ± (50 uV / Z_{ext})
10 – 45 Hz, 850 – 1MHz Accuracy	±0.1% of reading ±0.1% of range ± (0.02 * F)% of reading ± (50 uV / Z_{ext})
DC Accuracy	±0.1% of reading ±0.1% of range ± (100 uV / Z_{ext})

  - Thermal imaging camera (Flir One)

Parameter	Specification
Resolution	640 x 480 VGA (visible)
Temperature measurement	-20 to 120°C (-4 to 248°F)
Sensitivity	0.1°C (0.18°F)

  - Spectrum analyser (Rigol DSA815)

Parameter	Specification
Frequency range	9kHz to 1.5GHz
Frequency resolution	1Hz

  - Programable AC source (Keysight AC6801A)

Parameter	Specification
AC voltage output	
Rated voltage range	1 to 135 V_{RMS}/2 to 270 V_{RMS}
Voltage setting accuracy	0.3% of full scale/0.25% of full scale
Frequency	
Frequency setting range	40 to 500Hz
Frequency accuracy	±0.02%