# A Low-Profile, High Power Density Inverter with Minimal Energy Storage Requirement for Ripple Cancellation

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***Abstract*—An inherent characteristic of a Single-Phase Inverter is the DC-link voltage ripple. In order to ensure Maximum Power Point Tracking (MPPT) in Photovoltaic (PV) systems, the voltage ripple needs to be suppressed through use of an energy buffering device which can be a passive, i.e. typically a capacitor or active in the form of an Active Power Filter (APF). This paper describes a novel approach to an APF through a combination of hardware and software advances, with an emphasis on: a) further efficiency improvements through enhanced control; b) maximized deployment capabilities - the proposed APF is independent of the Inverter and can directly replace the DC-link ripple capacitor; c) high quality ripple cancellation; d) minimum storage capacitance.**

***Keywords—Active Power Filter; Inverter; Ripple Cancelation; Multilevel Converter; High Power Density;***

## I. INTRODUCTION

Various kinds of existing single-phase inverter system topologies have been explored in the literature [1][2]. These have been classified into single-stage and multi-stage inverters. Multi-stage inverters can be further classified into DC-DC-AC, DC-AC-DC-AC, and DC-AC-AC. Based on the location of the decoupling capacitor and circuitry, three decoupling techniques can be identified [3]:

- PV side decoupling
- DC-Link decoupling (focus of this work)
- AC side decoupling

Having the power decoupling capacitor on the PV panel side requires a very large capacitance value since the allowable voltage ripple must be fixed in order to an achieve efficient MPPT process. For the topologies with DC-DC-AC configurations, the first power stage is usually used to boost the low PV voltage to a high DC-Link voltage level compatible with the grid voltage. Placing the capacitor on the DC-Link allows for a much better use of capacitor energy storage. Because there is more energy stored at a higher voltage, required capacitor size is much lower and higher voltage in turn requires less current to provide equivalent power compensation, hence higher converter efficiency is potentially possible to achieve.

The capacitor can be one of the main lifetime limiting components in the system so that reduction of its size to the point which permits the use of non-electrolytic capacitors is beneficial. In this regard, a very effective approach by [4] achieves an impressive µF/W requirement for DC-Link ripple compensation. The power decoupling capacitor is also the biggest factor influencing inverter power density. For example, the Google's Little Box Challenge (LBC) [10], a competition for increasing power density of an inverter, resulted in different approaches to Inverter and APF topologies with one of the main goals being the reduction of the size of the power decoupling capacitor. Many attempts, including the finalists, have employed an APF approach equivalent to DC-DC-AC DC-Link decoupling.

Although APF approaches generally reduce the size of capacitor required, they introduce extra losses and therefore reduce the overall system efficiency. Also, the most common control approaches share a common characteristic – the APF and the Inverter control and hardware are typically closely coupled. Although existing solutions have been proven and deployed in real world applications with successful operation and good performance, these solutions are rigid in terms of system flexibility. The work presented in this paper aims to develop an APF independent of Inverter topology and control such that the APF could be used as a "plug and play" power decoupling device, that can directly replace the DC-Link decoupling capacitor, therefore liberating the designer's choice in Inverter topology.

## II. MULTILEVEL-BASED BUS RIPPLE FILTER AND CAPACITIVE STORAGE OPTIMISATION

### *A. Inverter system*

For the purposes of testing the APF the inverter system as illustrated in Fig. 1 is used in this work. This inverter is designed for PV cells which feed a DC/DC boost stage with MPPT. The APF and the Inverter are connected to the DC-link in parallel. All three modules are designed for 400 V DC-link

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operation. The APF hardware is a four-level flying capacitor synchronous buck/boost converter illustrated in Fig. 2. For development of the APF in this paper, the MPPT stage has been emulated by a DC voltage source with a 10 Ω resistor in series feeding the DC-link. This is comparable to the test setup suggested by LBC specifications. The Inverter stage has a similar topology to the APF with the addition that the buck/boost is followed by an unfolding bridge in order to achieve the AC output. Only islanded mode of operation is considered for the inverter.

### B. *Four-level buck/boost converter as a power pulsating buffer*

The four-level flying capacitor configuration in Fig. 2 allows for greatly reduced inductance values, reduced component stress and improved efficiency over a conventional synchronous boost/buck converter [5]. The technology has been proven at high power/voltage levels and the benefits it provides if adopted in medium voltage applications will enable a new generation of power converters [6]. The three FET pairs (Q1:Q6, Q2:Q5, Q3:Q4) are switched in complementary fashion using alternate modulation scheme [7], with each pair having a 120° phase offset. Alternate modulation allows for reliable average inductor current sampling and improved current control stability. The converter is capable of sinking and sourcing current to and from the energy storage capacitor in order to compensate the DC-link voltage ripple. With duty cycle limits of 0.05 and 0.95 and DC-link voltage of 400V, the available capacitor voltage ranges from 20 V to 380 V.

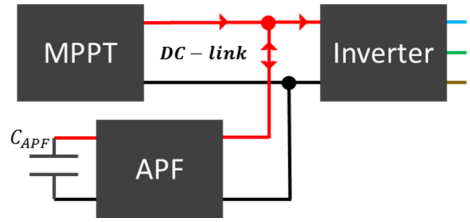


Fig. 1. Inverter system diagram described in this paper with: Maximum Power Point Tracking (MPPT) block; Inverter block including Unfolding Bridge (UFB) ; and Active Power filter (APF) block;

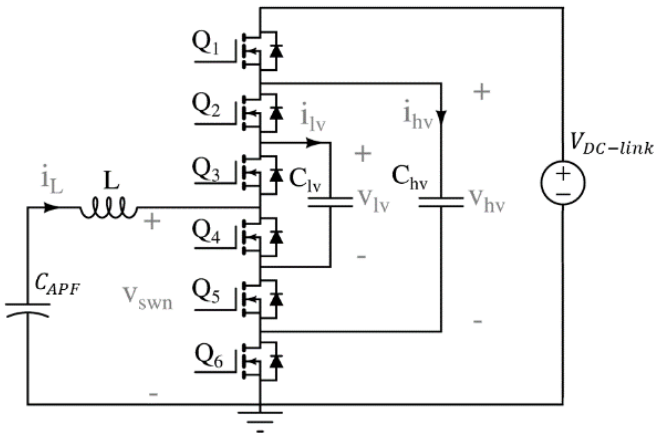


Fig. 2. Four-Level, flying capacitor synchronous buck/boost converter used as APF.

### C. *Capacitor calculation*

The power through the Inverter and APF and the energy required for compensation can be calculated as shown in [5]. Using the capacitor energy equation and $E_{INV}$ (the energy in the Inverter over one AC half-cycle) it is possible to derive (1) for calculating the capacitance required, for chosen APF capacitor voltage limits ($V_{MIN} - V_{MAX}$) and AC line frequency.

For compensating a 60 Hz, 2 kVA inverter, for chosen $C_{APF}$ voltage limits, using (1) it is possible to obtain a plot for capacitance required for $V_{min}$ in the range of $20\ V < V_{MIN} < 360\ V$ and $V_{MAX} = 380\ V$, as in Fig. 3. Because there is very little energy stored below $100\ V$, for this APF design voltage limits of $V_{MIN} = 100\ V$, $V_{MAX} = 380\ V$, were chosen which yields $C_{APF} = 79\ \mu F$. Adding tolerance, considering roll-off effects [8] and allowing for control headroom adds up to a nominal value of $150\ \mu F$, for compensating the DC-link ripple of a 60 Hz, 2 kVA inverter. The tolerances will depend on capacitor type and many other effects. Also, as pointed out by [4], an extreme case for inverter system operation is at 85°C therefore the effects described in [8] should be carefully considered to maintain stable APF operation throughout the operating temperature range.

$$C_{APF} = \frac{2E_{INV}}{({V_{MAX}}^2 - {V_{MIN}}^2)} \qquad (1)$$

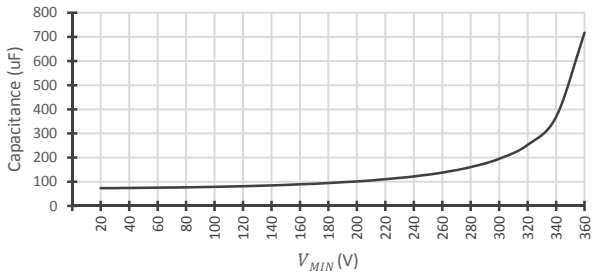


Fig. 3. $C_{APF}$ curve for different values of $V_{MIN}$ for $V_{MAX} = 380\ V$ in order to compensate 120 Hz DC-Link ripple for a 2kVA Inverter.

## III. CONTROL AND EFFICIENCY IMPROVEMENT

The proposed Multi-Loop control for the APF is illustrated in Fig. 4. The outer loop controller is a capacitor voltage stabilisation and steering (SSC) controller which runs on every peak/trough in the capacitor bank voltage, and maintains the capacitor voltage at a specified level regardless of the ripple amplitude. The inner controller is the ripple cancelation controller (RCC) which suppresses the DC-Link ripple by programming average inductor current to be injected into the DC-Link.

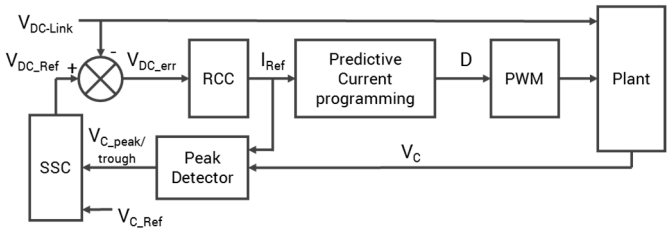

Fig. 4. Multi-Loop APF Control block diagram.

### A. DC-Link Ripple Cancelation Controller (RCC)

The main control objective is to regulate the DC-link voltage around a setpoint. This is achieved (using a PI controller) by calculating the current necessary to bring the DC-link voltage to the set point. Therefore, discrete PI error and integral terms are as described by equations (2) and (3). The overall controller is as per equation (4) below where *h* and *k* are proportional and integral gains respectively.

$$V_{DC\_Err}(t) = V_{DC\_Ref}(t) - V_{DC}(t) \tag{2}$$

$$Int_{DC}(t) = Int_{DC}(t-1) + V_{DC\_Err}(t) \tag{3}$$

$$I_L(t+1) = (V_{DC\_Err}(t)h + Int_{DC}(t)k)G \tag{4}$$

This controller has a fixed overall gain *G* and because of the non-linear energy storage nature of the capacitor bank, the suppressed ripple on the DC-Link is a distorted version of a sine wave. Because the peak of the DC-Link ripple corresponds to the trough in the capacitor, by incorporating an inverse of capacitor voltage into the overall gain of the controller, cancelation performance can be further improved. Then the final version of the controller is given by (5) below. For the capacitor voltage range of 100V – 380V then the gain will vary in the range of 1 – 3.8.

$$I_L(t+1) = \left(V_{DC\_Err}(t)h + Int_{DC}(t)k\right)\frac{V_{C\,MAX}}{V_C(t)}G \tag{5}$$

### B. Capacitor Voltage Limits

The $C_{APF}$ voltage limits chosen above, must be enforced to aid control and prevent duty cycle saturation. This is achieved by limiting current flow in the capacitor in a relative direction. If the upper voltage limit is reached, the current is only allowed to flow out of the capacitor. Similarly, when capacitor voltage reaches the lower limit, current is only allowed to flow into the capacitor. Every time the $C_{APF}$ voltage reaches the limits, the DC-Link reference is adjusted linearly i.e. the DC-Link reference is incremented at the upper limit and decremented at the lower limit. It is worth noting that at these two points the DC-link is out of regulation until the capacitor current changes direction, however these conditions serve to synchronise the APF with the Inverter (i.e. offset APF power by 180° compared to the Inverter) and are only present under load transients.

The limits are implemented in two stages, namely Soft Limit and Hard Limit. When the capacitor voltage reaches the Soft Limit the DC-Link reference is adjusted and the RCC resets but allows the system to continue. Hard Limit adjusts the DC-Link reference, resets the RCC and programs constant current to bring the capacitor voltage back inside the limits. Soft Limits prevent sharp current changes and 'soften' the system response. In the absence of any further capacitor voltage stabilisation control, this approach results in capacitor voltage bouncing between the limits as illustrated by measurements taken on APF hardware scaled for 40V operation - Fig. 5. The bouncing in capacitor voltage results in increasing and decreasing capacitor peak current. As the capacitor voltage drifts down, the peak current increases. Also the steps in DC-Link voltage are visible at the capacitor voltage limits.

The effectiveness of the limits to reverse the capacitor drift slope is very low and depends on the power imbalance. However, in the complete implementation the transients are handled by the Capacitor Stabilisation and Steering Controller (explained later) and the limits serve as a precautionary measure.

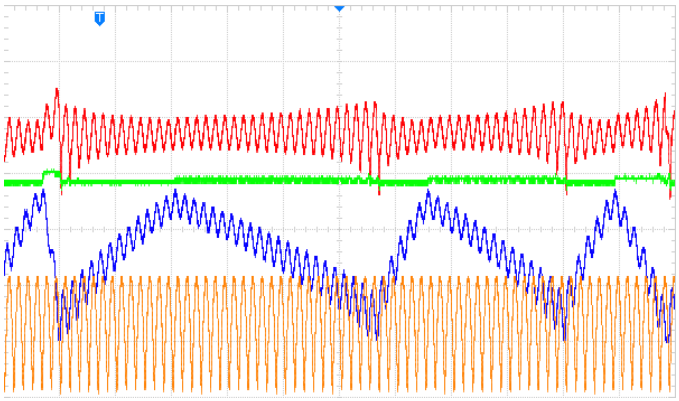

Fig. 5. Capacitor Voltage bouncing between the limits with no voltage stabilisation or steering. Note: the system is scaled to 40V operation. Capacitor Voltage (blue); Rectified inverter output (orange); DC-Link (green); Capacitor current (red); Horizontal axis – 50ms/div; Vertical axis – 10V/div;

### C. Capacitor Stabilisation and Steering Controller (SSC)

Conduction loss is directly related to current in the converter. Typically, the $C_{APF}$ voltage does not utilize the full voltage range. Therefore, by actively steering the capacitor voltage upwards to ensure that the voltage peaks are close to $V_{MAX} = 380\ V$ it is possible to maximise efficiency throughout the full operating power range of the system. Should the capacitor voltage be allowed to drift down such that $C_{APF}$ voltage troughs reach the lower limit $V_{MIN} = 100\ V$, the conduction loss will be increased. For an illustrative case where three FETs will be on at any given instance with $R_{DS\_ON}$ of 50 mΩ and an inductor resistance $R_L$ of 100 mΩ, and considering peak capacitor current throughout the power range it is possible to estimate conduction loss for the APF topology outlined by Fig. 2. Fig. 6 illustrates the estimated conduction loss for worst case (capacitor allowed to operate at the lowest voltage), maximum power case (capacitor is always biased at a point which accommodates maximum power) and ideal case (capacitor peaks are held at maximum available voltage). Clearly there is a significant advantage in terms of conduction loss by ensuring that capacitor voltage is always maintained at its maximum level. The increased current which gives rise to the increased conduction loss at lower capacitor voltage can also be observed earlier in Fig. 5.

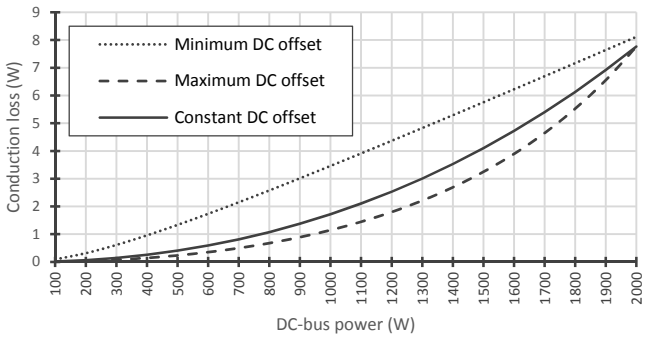


Fig. 6. Calculated APF Conduction loss with different levels of capacitor voltage DC offset over the operating power range. Note: Constant DC offset refers to a level that accommodates maximum power.

Where there is a continued power imbalance between APF and Inverter stages, the $C_{APF}$ voltage will saturate either high or low depending on whether the net power is positive or negative. From this, a secondary control objective arises - the DC-link reference voltage needs to be adjusted (directly related to energy) in order to achieve quasi-steady capacitor voltage operation. The DC-link reference voltage control is based on $C_{APF}$ peak and trough values using an equation derived from capacitor energy. Three cases can be considered as follows:

- CASE 1 - If the reference level is too high, the APF will try to supply a DC current to maintain the DC-Link voltage (as well as AC current cancelling the ripple) which will eventually drain the capacitor.
- CASE 2 – If the reference level is too low, the APF will try to consume a DC current to maintain the DC-Link voltage (as well as AC current cancelling the ripple) which will eventually saturate the capacitor.
- CASE 3 – Ideal situation will result in zero DC current with only the AC ripple cancelling current present and capacitor voltage peaking at reference level.

Fig. 7 illustrates the capacitor voltage for the case that the DC voltage reference level is set too high and as a result the capacitor begins to drain.

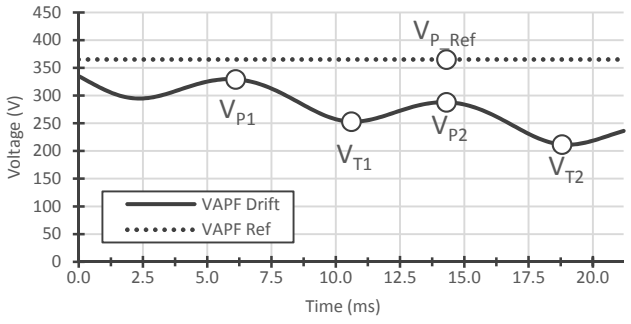


Fig. 7. Capacitor Bank voltage peaks (P1, P2), troughs (T1, T2) and peak reference (Pref).

Considering the three cases and the objectives to control capacitor voltage drift under transients and conduction loss minimisation, using Fig. 7 a set of equations can be derived based on capacitor energy. The change in energy between peaks $V_{P1}$ and $V_{P2}$ or troughs $V_{T1}$ and $V_{T2}$ during a period $T_{2\omega}$ is described as (6) and (7). Similarly, the change in energy required to bring the latest peak to the reference level is described by (8).

$$E_C = \frac{1}{2}C\left({V_{P1}}^2 - {V_{P2}}^2\right) \tag{6}$$

$$E_{C'} = \frac{1}{2}C\left({V_{T1}}^2 - {V_{T2}}^2\right) \tag{7}$$

$$E_0 = \frac{1}{2}C\left({V_{P\_Ref}}^2 - {V_{P2}}^2\right) \tag{8}$$

Also, the energy on DC-Link side of the APF can be expressed as an integral of power over the same period $T_{2\omega}$ as in (9) where DC-Link voltage and APF inductor current are the average values over the period. Assuming that $V_{DC-Link} = V_{DC\_Ref}$ in steady state.

$$E_{DC\_Step} = V_{DC-Link}\, I_L\, T \tag{9}$$

The total step in energy to bring the capacitor peak to the reference level can be described as (10) for peak and trough cases respectively.

$$\begin{aligned} E_{C\_Step} &= E_C + E_0 \\ E_{C\_Step'} &= E_{C'} + E_0 \end{aligned} \tag{10}$$

Equating (9) and (10) to obtain an expression for a step in DC-Link reference voltage yields (11).

$$\begin{aligned} V_{DC\_Step} &= M\left({V_{P1}}^2 - 2{V_{P2}}^2 + {V_{P\_Ref}}^2\right) \\ V_{DC\_Step'} &= M\left({V_{T1}}^2 - {V_{T2}}^2 + {V_{P\_Ref}}^2 - {V_{P2}}^2\right) \\ where\ M &= \frac{C}{2\, I_L\, T} \end{aligned} \tag{11}$$

Considering a fixed period of operation, maximum peak current through the capacitor and the capacitance value, *M* can be simplified to a constant to accommodate maximum power level. Then in CASE 3 (11) will evaluate to zero and in all other cases as a step in DC-Link reference voltage. Therefore, this non-linear control equation can be thought to have similar behaviour to incremental PI. Introducing the current DC-Link reference level into the equation, produces the required absolute output as in (12). The following equations are intended for use at peak and trough detection respectively.

$$\begin{aligned} V_{DC\_Ref}(t_{2\omega} + 1) = {} & V_{DC\_Ref}(t_{2\omega}) \\ & - M\left({V_{P1}}^2 - 2{V_{P2}}^2 + {V_{P\_Ref}}^2\right) \end{aligned} \tag{12}$$

$$V_{DC\_Ref}(t_{2\omega}+1) = V_{DC\_Ref}(t_{2\omega}) - M\left({V_{T1}}^2 - {V_{T2}}^2 + {V_{P_{Ref}}}^2 - {V_{P2}}^2\right)$$

$NOTE$: $t_{2\omega}$ *is the sampling time corresponding to period between capacitor peaks/troughs*

It is worth noting that the DC-Link reference level should have a limited range with the lower limit capable of accommodating the maximum power situation and the upper limit being maximum safe operating point. This is because of the nature of voltage limits on capacitor bank. As described above, the DC-Link reference is incremented/decremented when the capacitor voltage reaches the upper/lower limits respectively.

## IV. SIMULATIONS AND RESULTS

### *A. RCC performance*

Earlier in section III.A it was suggested that the introduction of a variable gain for the RCC PI control would be more effective at reducing ripple. Here we compare the results for a fixed gain G in (4) and a variable gain under two different inverter power levels. Simulating the RCC with a fixed overall gain of 1 suggests that ripple cancelation performance degrades as DC-Link ripple increases. Fig. 8 and Fig. 10 show RCC performance under two different power conditions. In Fig. 10 under more power, the case is exaggerated as the peaks get sharper and the suppressed ripple is not sinusoidal anymore. This can be related to the non-linear energy storage in the capacitor where peak of the ripple on the DC-Link corresponds to the trough of the capacitor ripple (which is at a considerably lower voltage). Because the gain is fixed and there is less energy at lower voltage, the ripple cancelation is not as effective.

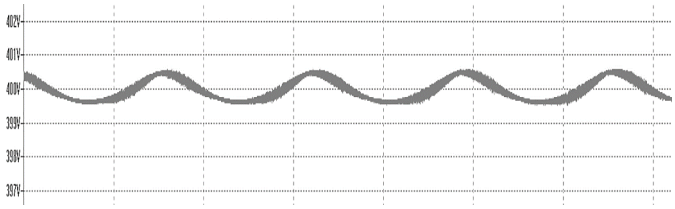

Fig. 8. RCC with fixed overall gain of 1. Supressing 40Vp-p ripple @ 120Hz. 1V/div;

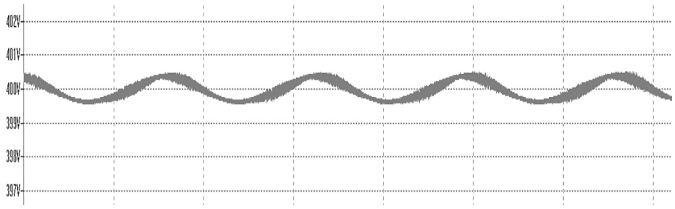

Fig. 9. RCC with variable overall gain. Supressing 40Vp-p ripple @ 120Hz. 1V/div;

This implies that boosting the gain during capacitor troughs should reduce the ripple peaks on the DC-Link. The inverse of capacitor voltage can be employed to achieve the desired variable gain as described by (5). The positive effect is modest at lower power, Fig. 8 vs. Fig. 9, but becomes clearly visible at larger power levels as illustrated by Fig. 10 vs. Fig. 11 where each set of figures illustrate before and after performance respectively.

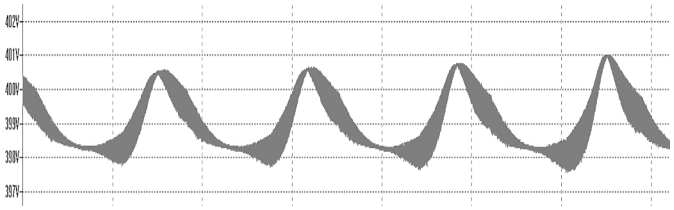

Fig. 10. RCC with fixed overall gain of 1. Supressing 80Vp-p ripple @ 120Hz. 1V/div;

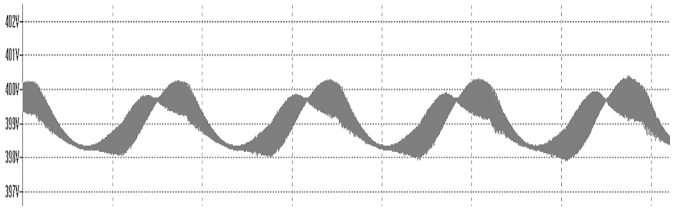

Fig. 11. RCC with variable overall gain. Supressing 80Vp-p ripple @ 120Hz. 1V/div;

Fig. 12 and Fig. 13 illustrate RCC performance implemented in hardware with fixed and variable gain respectively. Although the higher frequency components dominate the overall ripple amplitude, the variable gain RCC further reduces the low frequency DC-Link ripple and provides a more uniform suppression.

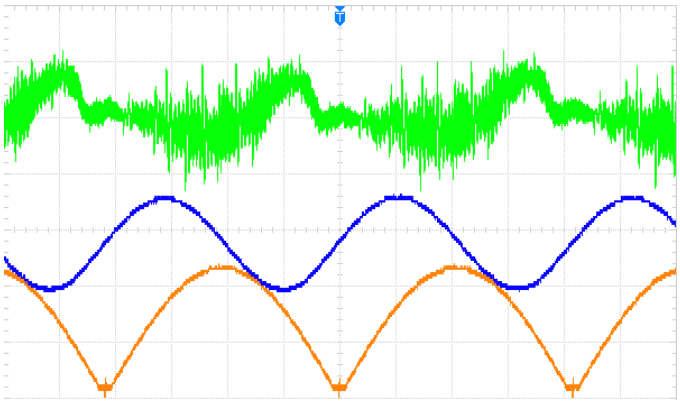

Fig. 12. RCC with fixed gain compensating 500W DC-Link ripple @ 120Hz. 2ms/div; Capacitor Voltage (blue) 50V/div; Rectified inverter output (orange) 50V/div; DC-Link (green) 2V/div;

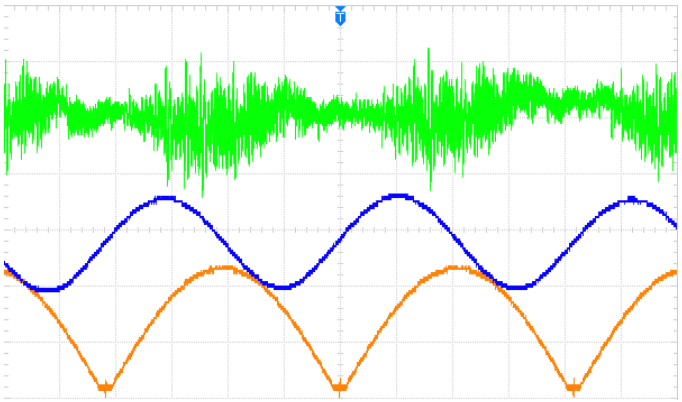

Fig. 13. RCC with variable gain compensating 500W DC-Link ripple @ 120Hz. Capacitor Voltage (blue) 50V/div; Rectified inverter output (orange) 50V/div; DC-Link (green) 2V/div;

### *B. Full voltage system performance*

LBC specifications require < 3% ripple on 450 V DC-Link with a 230 V 120 Hz Inverter. The prototype hardware was operated at 225 V DC-Link with a 115 V 120 Hz Inverter at 500 W. With SSC implemented and tested in hardware the capacitor voltage is stabilized and steady state operation is shown in Fig. 13. The remaining DC-Link ripple corresponds to ~2.1%.

Full load system startup, as illustrated by Fig. 14, only takes three AC cycles for APF to be in full operation. A 50% load step transient response is illustrated in Fig. 15. The extra capacitance for control headroom, mentioned earlier, is useful in maintaining DC-Link operation during transients while the DC-Link reference is recalculated by the SSC. Power imbalance between APF and Inverter stages may be caused by a few different however equivalent situations. These can arise either from change in Inverter load or change in MPPT power output. Both cases put the APF in the same situation – the calculated DC-Link reference voltage is either too high or too low which causes a drift in capacitor voltage. Fig. 16 and Fig. 17 illustrate the system responses to changes in DC-Link voltage. The system can handle changes in DC-link voltage, however the size of the step that can be handled depends on the amount of overdesigned capacitance to allow for capacitor voltage drift. In Fig. 17 the SSC cannot react in time and the capacitor voltage bottoms out at the lower limit causing the RCC to go out of regulation for two inverter cycles. This is an inherent drawback of this approach because the only indication in power change is the drift in capacitor voltage which is slow to detect. However, the APF is not the only device responsible for DC-Link operation. In a DC-DC-AC system the boost stage and Inverter should both react to changes in load much faster than the APF.

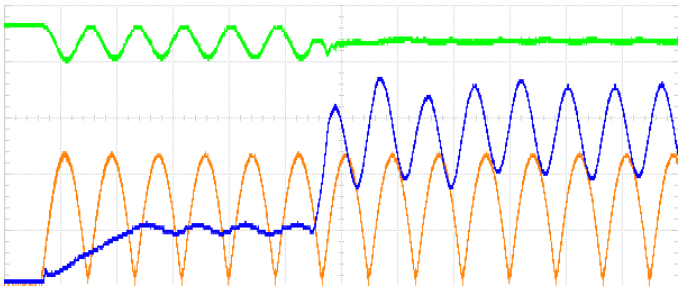

Fig. 14. Full load system start up. Capacitor Voltage (blue); Rectified inverter output (orange); DC-Link (green); Horizontal axis - 10ms/div; Vertical axis – 50V/div;

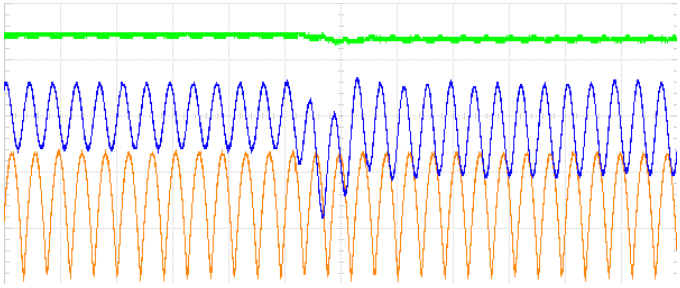

Fig. 15. Load step, 50% to 100%, transient response. Capacitor Voltage (blue); Rectified inverter output (orange); DC-Link (green); Horizontal axis - 20ms/div; Vertical axis – 50V/div;

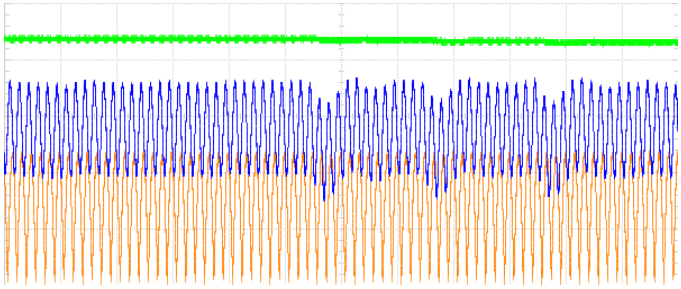

Fig. 16. DC-Link voltage three consecutive step downs of 1V (system running @ 500W). Capacitor Voltage (blue); Rectified inverter output (orange); DC-Link (green); Horizontal axis - 50ms/div; Vertical axis – 50V/div;

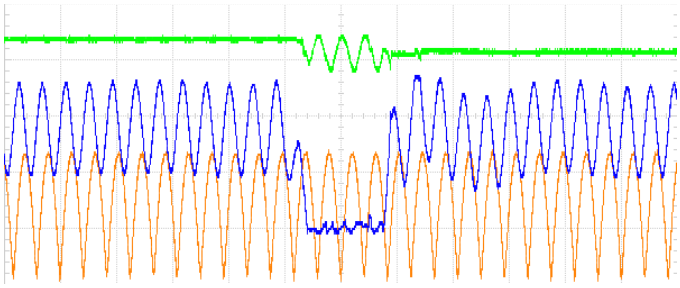

Fig. 17. DC-Link voltage step down 10V transient response (system running @ 500W). Capacitor Voltage (blue); Rectified inverter output (orange); DC-Link (green); Horizontal axis - 20ms/div; Vertical axis – 50V/div;

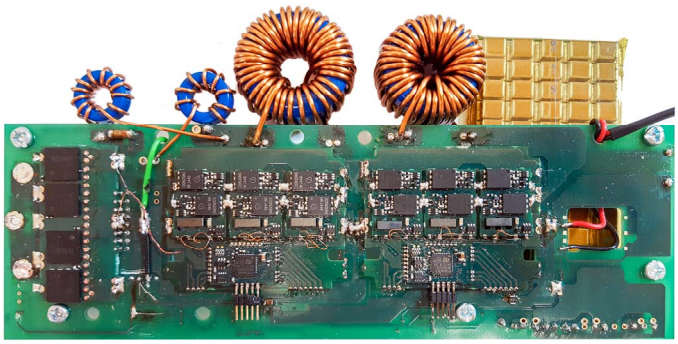

Fig. 18. Prototype hardware. Overall dimensions: 165mm x 85mm x 18mm.

## *V.* CONCLUSION

This work has demonstrated that the proposed approach of an independent APF can be a practical solution for DC-Link ripple cancelation with reduction in capacitor size, improved ripple cancelation performance, and increased reliability as compared to an electrolytic capacitor bank. Furthermore, adaptation of proven multilevel converter technologies brings advantages such as reduction in passive component size, reduction in cost and improved efficiency.

Existing APF solutions are interleaved/specifically designed for inverter topologies. This approach liberates the system designer's choice of inverter topology and reduces development time because the proposed APF can be applied to conventional multi-stage DC-DC-AC single phase inverters by directly replacing the DC-Link capacitor bank.

A simple PI controller with variable gain has proven to be an adequate solution for DC-Link ripple cancelation however potential performance gains may be obtained by a more advanced approach like Proportional Resonant controller [11].

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