99% Efficiency 3-Level Bridgeless Totem-pole PFC Implementation with Low-voltage Silicon at Low Cost

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***Abstract*— Achieving 99% efficiency for totem-pole PFC front-end stages with wide band gap (WBG) devices is no longer seen as a rare accomplishment. Design concerns revolving around the maturity of WBG technologies, the lack of dual sources, and very high component costs, lead to a quest for a medium-term low-cost mature silicon-based solution. Given poor reverse recovery performance associated with high-voltage (above 600V) Super-junction MOSFETs, existing approaches generally deploy boundary conduction mode (BCM) and interleaving for switching loss and EMI benefits. This makes control and system design relatively complex, costly, and as a result unattractive to cost-sensitive applications. Therefore, this article proposes a simple yet highly-efficient PFC implementation based on a 3-level bridgeless totem pole topology and 150V MOSFETs. The proposed solution is demonstrated in a complete 3kW PFC stage prototype in a compact form factor of 50mm x 260mm x 1U with an ultra-high efficiency exceeding 99% at 230V.**

Keywords—Power factor correction, multi-level, bridgeless, totem-pole, high efficiency.

I. INTRODUCTION

Power factor correction (PFC) functionality is a fundamental building block in all midrange AC/DC switched mode power supplies (SMPSs) for electronic equipment. Our work primarily relates to power levels from about 300W – below which efficiency rarely gets commercially rewarded – through to 3kW, which corresponds approximately to the limit for practical single-phase operation.

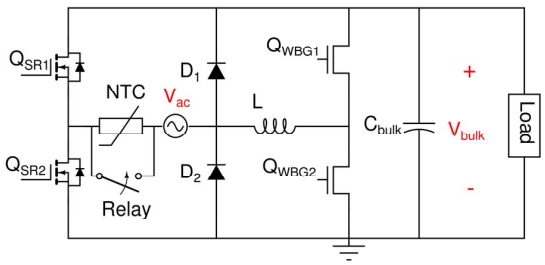


Fig. 1. Conventional bridgeless totem-pole PFC with line synchronous rectification

Minimizing conduction losses of PFC rectification is important for SMPSs to surpass Titanium efficiency level [1] and reduce heat generated during low-line operation, e.g. 100Vac. Various studies [2], [3], [4]. have pointed out the relevance of the bridgeless totem-pole arrangement for PFC applications. In a topology context, this is a very simple circuit as illustrated in Fig. 1. It also has the advantage of using a single PFC inductor as compared with the semi-bridgeless approach which requires a dual inductor.

Stacking of active switches Q_{WBG1} and Q_{WBG2} in Fig. 1 immediately rule out Silicon Super-junction technology due to long reverse recovery time and high reverse recovery charge Q_{rr}, causing extreme shoot-through current and associated losses. This is the main challenge to its usage and may explain the historical preference for conventional diode-bridge boost solutions in spite of high conduction loss due to extra diode drop in those bridge types as well as boost diodes.

Doing soft switching through BCM is one feasible option to overcome reverse recovery challenge. However, this typically requires complex control and system design – given the wide range of operating conditions – and as a result it is unattractive to cost-sensitive applications. Another downside of BCM operation is high differential-mode EMI noise at high input current and interleaving is generally required, which further complicates controller design. Therefore, continuous conduction mode (CCM) and hard switching seems to be the norm.

The logical approach to bridgeless totem-pole PFC implementation is to use devices with very fast or ideally no reverse recovery as the active switches [5], [6], and hence usage of wide band gap (WBG) devices such as GaN or SiC. The low capacitance of WBG devices assists in limiting losses under hard switching, albeit with challenges in dV/dt and dI/dt management.

Achieving 99% efficiency for totem-pole PFC front-end stages with wide band gap (WBG) devices is no longer seen as a rare accomplishment. Design concerns revolving around the maturity of WBG technologies, the lack of dual sources, and non-standard high-cost components, lead to a quest for a medium-term standard and low-cost silicon-based solution.

Given poor reverse recovery performance of Super-junction MOSFETs and complex control of soft switching, the only possible choice for silicon implementation is to use low voltage MOSFETs in multilevel power converters.

Multilevel conversion techniques have been used for some time in high-voltage and high-power DC-to-AC inverters and DC-to-DC choppers where a single switching device either is unable to handle a full voltage swing, e.g. over 5kV, or cannot provide adequate performance in terms of speed, efficiency, and EMI noises [7], [8]. The key benefit of multilevel power conversion is to use multiple

switches for evenly sharing the voltage stress, allowing the deployment of lower voltage rating but faster switching devices.

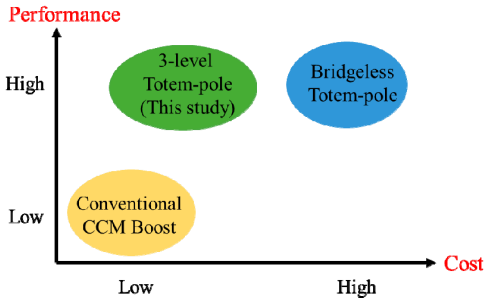


Fig. 2. Performance vs. cost benchmark for conventional and emerging PFC technologies

Recently, several studies have been conducted for single phase AC-DC rectifiers, but the main intention is on magnetic size reduction and extreme power density [9], [10], [11], [12] rather than on system cost and efficiency optimization. Therefore, this paper will focus on implementation of a 3-level variant of the topology proposed in [11] with main priorities of exceeding 99% efficiency and lowering system BOM cost. Fig. 2 benchmarks performance and cost for existing PFC technologies, and highlights the objective of this study.

II. 3-LEVEL BRIDGELESS TOTEM-POLE PFC OPERATION

Fig. 3 illustrates the schematic of the topology of interest which is technically derived from the 4-level bridgeless totem pole arrangement as proposed in [11] except that two thyristors are replaced with line synchronous rectifiers for conduction loss minimization. Managing inrush current during start-up is realized by an NTC thermistor which is subsequently bypassed by a relay during steady state for further conduction loss reduction. Two bypass diodes D_1 and D_2 provide an alternative low impedance path to the bulk capacitor C_{bulk}, preventing inrush current from going through the PFC inductor L and MOSFET string on startup or during input surge events. The inductor L, MOSFET string, and flying capacitor C_{fl} form a 3-level synchronous boost converter. Flying capacitor initialization is realized by a passive clamped circuit as discussed in [11] but it is not shown here for simplicity.

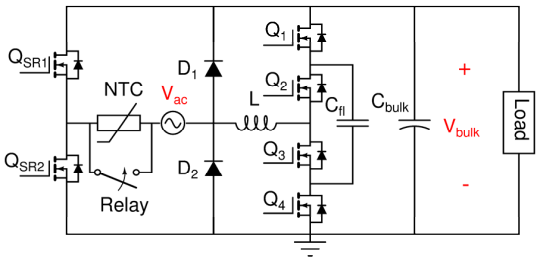
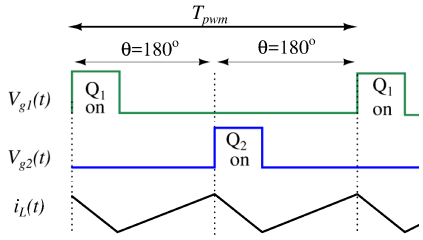
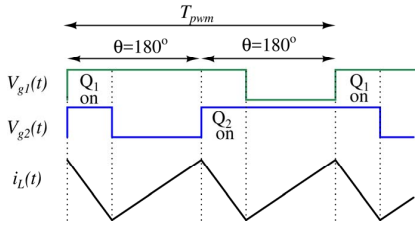


Fig. 3. 3-level bridgeless totem-pole PFC with line synchronous rectification. For clarity of presentation, EMI filters and diode clamp circuitry are not included in the diagram.

The circuit as shown in Fig. 3 inherits the operating principle of the conventional bridgeless totem pole PFC. Particularly, in the positive half line-cycle where Q_{SR2} is conducting and Q_{SR1} is off, the converter operates in a similar fashion as a synchronous boost converter with Q_3 and Q_4 being boost switches while Q_1 and Q_2 function as synchronous rectifiers feeding the bulk capacitor C_{bulk}. The operation in the opposing half line-cycle is also similar to that of synchronous boost converters; however, those switches swap their roles and the inductor current flows in a reverse direction.



(a) Duty ratio D < 0.5



(b) Duty ratio D > 0.5

Fig. 4. Phase-shift modulation and resultant inductor current waveforms of 3-level flying capacitor boost converters

The 3-level MOSFET string is driven in a phase-shift manner. In particular, Q_1 and Q_4 are paired, and it is done likewise for Q_2 and Q_3. Each pair of switches forms one phase and is complementarily driven, i.e. when one switch of the pair is on, the other must be off and vice versa. The control signals of Q_1 and Q_2 share the same duty ratio D and switching period T_{pwm}, but they are offset in phase by an angle of 180 degrees. Q_4 and Q_3 are driven by negating the driving pulses of Q_1 and Q_2, respectively. An example of the phase-shift modulation scheme for two different duty ratio values is illustrated in Fig. 4.

TABLE I. CAPACITOR VOLTAGE AND INDUCTOR CURRENT RELATIONSHIPS OF A 3-LEVEL BOOST PFC

	Positive line half cycle	**Negative line half cycle**
DC voltage gain $\frac{\lvert V_{ac}\rvert}{V_{bulk}}$	$1-D$	D
DC flying capacitor voltage V_{fl}	$\frac{V_{bulk}}{2}$	
Maximal inductor current ripple ΔI_L (peak-to-peak) at $D = \frac{1}{4}, \frac{3}{4}$	$\frac{V_{bulk} T_{pwm}}{16L}$	
Maximal flying capacitor voltage ripple ΔV_{fl} (peak-to-peak) at $D = \frac{1}{2}$	$\frac{I_L T_{pwm}}{2C_{fl}}$	

It is assumed that the converter stays in CCM during operation and its DC characteristics can be adequately modelled by ideal switches and passive components. Given those assumptions, one can derive steady-state voltage and current values as well as associated ripples by following the procedure as described in [11]. Main results of DC and ripple analyses are captured in TABLE I. The results confirm many attractive characteristics of multilevel power conversion.

- Inherent frequency multiplication where each phase switches at a low frequency with the effective frequency being a multiple of the phase frequency.
- Low-voltage switching where each phase is switched at voltage levels much lower than the PFC output voltage, e.g. $V_{bulk}/2$ for 3-level implementation. Alongside the low switching frequency property as cited above, this can result in very efficient operation with low switching losses.
- Inherently lower dV/dt and dI/dt are of value in limiting EMI/EMC effects.
- The topology operates with phase cancellation, implying reduced voltage applied to the PFC inductor for reduced time. As inductor size tends to be a function of applied volt-seconds, there is the opportunity for making this key component smaller and neater as compared with the conventional (2-level) implementation. For example, for the same current ripple, the discussed 3-level bridgeless topology requires four times less inductance than the conventional boost converter, or equivalently four times less stored energy/volume for the same power rating.

III. Low-cost Isolated Gate Driver

Driving multiple high-side MOSFETs requires isolated gate drive techniques with precise channel matching for reliable operation and voltage balance of flying capacitor multi-level converters. Since most commercial isolated driver ICs are quite costly and often need a floating supply on the switch side, relying on them for multilevel implementation could be technically possible but commercially impractical, particularly for single phase applications. Fortunately, this cost concern can be fully addressed by deploying innovative gate drive technologies developed and patented by ICERGi [13] with key benefits of low component counts, low cost, and most importantly obviating the need for local power supplies.

The operating principle is simply magnetic coupling with ferrite cores, allowing simultaneous transmission of both drive signal and power on the same channel. However, unlike conventional transformer-coupled PWM gate drive approaches [14], the proposed circuit in [13] is innovatively designed to work with miniature magnetics enabling a compact implementation with full galvanic isolation at much lower cost.

The basis of operation is that pulses are first generated, corresponding to the edges of PWM signals as illustrated Fig. 5. Those pulses are then amplified and correspondingly sent to separate ON and OFF transformer-coupled channels with capabilities of transferring both drive information and energy. At the outputs of the ON and OFF transformers, pulses with energy are fed to a monostable circuit which instantaneously pull the gate of driven device high or low depending on pulse types as shown in Fig. 5.

The monostable multi-vibrator has limited reset time to protect driven devices from latching conditions. For operating time longer than the reset period, the digital circuit on the control side of the driver will send refreshing pulses to reinitialize the monostable operation and drive voltage.

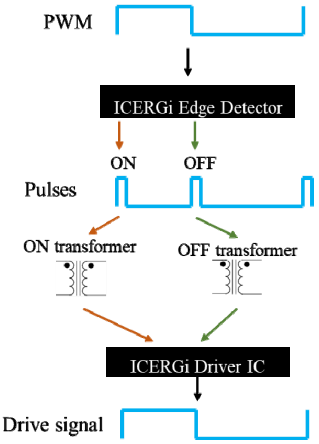


Fig. 5. Pulse generation and direct drive transmission principle

ICERGi have developed a unique approach to transformer implementation allowing resource sharing between two drive channels. This results in tiny magnetics with low intrinsic cost, high common mode noise immunity, and most importantly inherent inter-lock capability, i.e. no cross conduction between two driven devices.

The input-to-output propagation delay is the aggregation of delays in the edge detector and monostable multi-vibrator. The former quantity could be dominant depending on Silicon technology implementation and cost. One effective approach to propagation delay and cost reduction is to replace the edge detection process with direct ON and OFF pulse generation using digital control. The approach has been successfully demonstrated in various PFC and LLC converter designs including this study.

IV. Series-connected MOSFETs and Voltage Sharing

Phase-shift modulation naturally forces the flying capacitor C_{fl} into settling around $V_{bulk}/2$ at steady state as confirmed in TABLE I. , meaning that operating voltage of active switches Q_1, Q_2, Q_3, and Q_4 should be a half of the output voltage V_{bulk}, particularly 200V for a nominal output of 400V. Practical implementation requires 50% margin, which suggests 300V-rating MOSFETs.

Existing commercial 300V devices have a very limited choice of on-state resistance and unattractive switching characteristics as compared to lower voltage counterparts. TABLE II. shows a side-by-side comparison of 300V- and 150V-type MOSFETs from the same manufacturer. Differences in reverse recovery performance and on-state resistance are significant even though two part-types have the same packaging. This suggests that replacing a 300V-rating MOSFET with two 150V ones in series could allow

considerable reduction in both switching and conduction losses, which is key to ultra-high efficiency and power density. The rest of this section will discuss a solution of forming a composite 300V switch by connecting two 150V-rating MOSFETs in series and driving them ON and OFF simultaneously with minimal time offset, e.g. less than 1ns.

TABLE II. FIGURE OF MERIT (FOM) COMPARISON BETWEEN 300V AND 150V MOSFETS

	300V SuperSO8 BSC13DN30NSFD	**150V SuperSO8 BSC110N15NS5**
On-state resistance R_{DSON}	130mR	11mR
Reverse recovery time t_{rr}	111ns	45ns
Reverse recovery charge Q_{rr}	249nC	46nC
Output charge Q_{oss}	48nC	78nC
Gate charge Q_g	23nC	28nC

Stacking two low-voltage MOSFETs in series in order to achieve a higher voltage rating has been well considered in industry. Main concern is voltage sharing between two devices during normal operation as well as transient responses. If one MOSFET is switched off before the other, it may be subjected to blocking a voltage greater than its rating, causing reduction in the device life time. Therefore, managing voltage sharing all comes down to how closely two MOSFETs are driven and their intrinsic drain-to-source capacitance which generally acts as a voltage divider.

- If the same component type from the same manufacturer is used, it is unlikely that the tolerance in parasitic capacitance will cause any significant difference between drain-source voltages of series-connected MOSFETs.
- Having low-cost isolated gate drivers with precise matching for series-connected devices is important to ensure voltage sharing

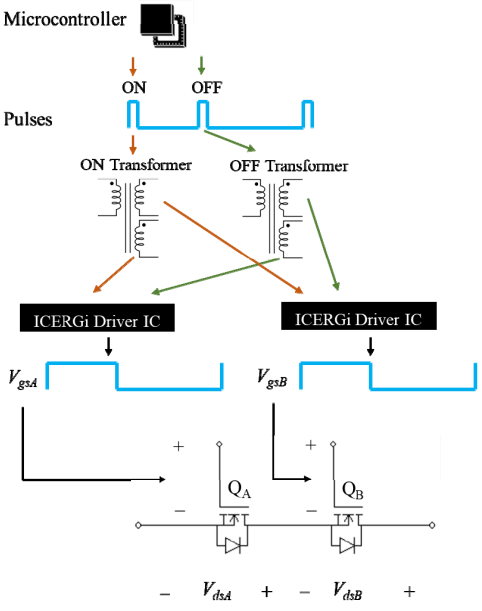
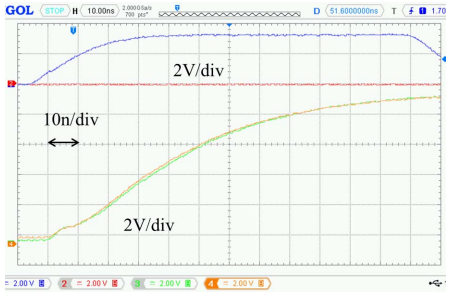


Fig. 6. Proposed isolated drive solution for two series-connected 150V MOSFETs

If two 150V devices of a composite switch are assumed to possess similar turn-on and turn-off characteristics, driving them simultaneously can be achieved by cloning drive pulses using multiple output transformers as illustrated in Fig. 6. Specifically, both ON and OFF transformers as mentioned in III are modified to have two isolated outputs, each will feed a separate ICERGi drive IC which is required to reconstruct PWM signals from pulses. Time offset between two outputs could be minimized by using planar windings with symmetrical structures. Having small magnetic sizes also help improve delay matching by allowing greater control of leakage inductance.

(a) Gate drive delay matching – 70kHz switching frequency



(b) Detailed turn-on delay matching

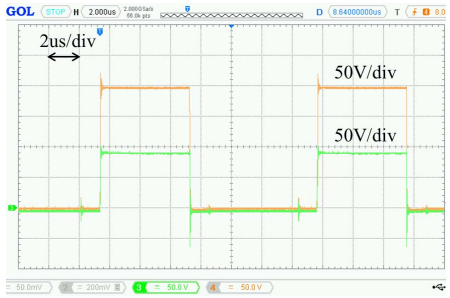
(c) Detailed turn-off delay matching

Fig. 7. Gate drive waveforms of two series-connected 11mR 150V MOSFETs (BSC110N15NS5): BLUE – ON pulse, RED – OFF pulse, GREEN – V_{gsA}: Drive voltage of Q_A, ORANGE - V_{gsB}: Drive voltage of Q_B

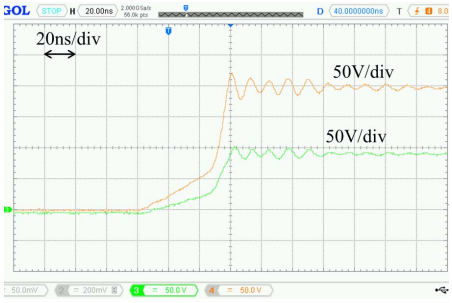
Fig. 7 shows experimental drive waveforms of two MOSFETs in series along with ON and OFF pulses output by a microcontroller. Pulse width is the same for both types and set to 120ns. By studying turn-on and turn-off transitions in detail, one can confirm that two drive channels are almost

identical and have minimal time offset, i.e. much less than 1ns. Slight offset in pull-down voltage levels occurs during off state but this should have no effect on either voltage sharing or device life span. Drive voltage during ON and OFF transitions seems to be very clean and healthy, i.e. monotonic increase/decrease with no visible sign of a Miller plateau region.

Another interesting observation in Fig. 7 is that the propagation delay from the microcontroller to MOSFETs is quite short. The worst case is at turn-off and this is still less than 10ns. This feature is highly beneficial to applications running at MHz frequencies.



(a) Switched waveform with a fixed frequency of 70kHz



(b) Detailed turn-off transition

(c) Detailed turn-on transition

Fig. 8. Voltage sharing between two series-connected 11mR 150V MOSFETs (BSC110N15NS5): GREEN – V_{dsA}: Voltage across Q_A, ORANGE – $V_{dsA} + V_{dsB}$: Voltage across Q_A and Q_B

Voltage sharing is evaluated by looking at drain-to-source voltage waveform across two bottom MOSFETs of a 3-level bridgeless PFC prototype operating at 400V output. It can be confirmed that voltage stress is shared evenly between two devices during normal operation as shown in Fig. 8 and during transient responses, e.g. start-up, step loads, etc…. Experimental data for later scenarios also show similar responses as found in Fig. 8, hence they are not included in this paper.

Thanks to outstanding reverse recovery performance of 150V MOSFETs, both turn-on and turn-off actions are clean with minimal ringing (waveforms are captured without bandwidth limit). This indicates low switching loss and EMI noises.

For both experiments as captured in Fig. 7 and Fig. 8, two 150V devices under test are the same type, i.e. 11mR SuperSO8 Infineon OptiMOS BSC110N15NS5, but come from different manufacturing batches.

V. Digital Control and Drive Implementation

By obviating the need for local power supplies as typically required in commercial isolated driver ICs, the technology as presented in III and IV allows driving of multilevel switches with low component count and at low cost, enabling integration of drive and control into a single PCB board.

A low-cost commodity ARM Cortex M0-based digital controller can work well in control of multilevel converters and is designed for optimal usage of the driver characteristics.

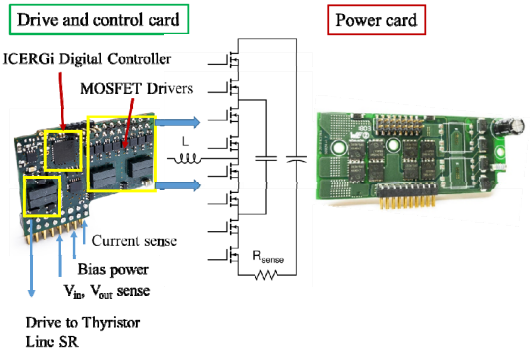


Fig. 9. Integrated drive and control card for 3-level flying capacitor boost converters. It can couple with a power board, forming a module intended for vertical mounting on a main PCB board.

Fig. 9 shows a low-cost component-type daughter board with a digital controller and 8 isolated drivers for the MOSFET string. The digital controller can be programmed for different end applications other than PFC. This approach has allowed the inherent advantages of multilevel technologies to be realised in a practical and cost-effective fashion at relevant power levels, typically the 300W→3kW range as needed for most of the single-phase marketplace.

The drive and control card has several pin-outs for current and voltage sensing as well as drive purposes.

For PFC implementation, a fully digital control algorithm as proposed in [15] is implemented in the ARM M0 microcontroller. In addition to basic functionalities, most protection as typically found in PFC analogue controllers and standard communications with down-stream stages are also included in the firmware.

VI. Experimental Results and Discussion

A prototype is designed to meet specifications as listed in TABLE III.

TABLE III. Converter Design Specifications

Universal line voltage, V_{line}	$85V_{ac} - 265V_{ac}$
Nominal output voltage, V_{bulk_nom}	$400V_{dc}$
Hold-up time, T_{holdup}	16ms @ 3kW
Switching frequency, f_{pwm}	70kHz
Maximal output power, P_{out_max}	3kW @ $230V_{ac}$ 1.5kW @$115V_{ac}$
Maximal pk-pk flying capacitor voltage ripple ΔV_{fl}	20V
Maximal pk-pk inductor current ripple ΔI_L	1A

Calculations suggest the following component values: L= 400uH, C_{bulk} = 990uF – 450V rating- electrolytic type, C_{fl} = 12uF – 450V rating – film and ceramic type . The main 150V power switches are BSC110N15NS5 with drain-source on-state resistance of 11mΩ while line synchronous rectification uses 650V 19mR MOSFETs IPW65R019C7. Fig. 10 shows complete 3kW PFC hardware implementation including a 2-stage EMI filter and a 5W bias supply.

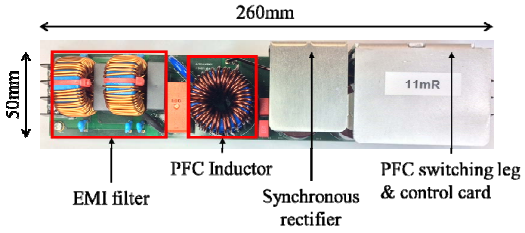


Fig. 10. 3kW PFC hardware prototype in 50mm x 260mm x 1U

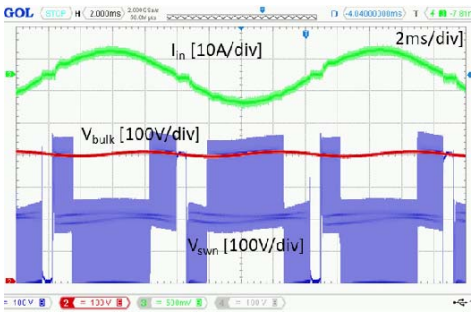


Fig. 11. Operational waveforms at 230Vac and 1.5kW output load: GREEN – Input line current, PURPLE – Switched node voltage, RED – Bulk capacitor voltage

Voltage and current waveforms captured at 230Vac and 1.5kW resistive load are presented in Fig. 11. The switched node voltage shows steps of 200V which is well within the aggregate voltage rating of two series-connected MOSFETs. Fig. 11 also confirms that the converter operates in a stable manner with no sign of voltage imbalance, which proves the feasibility of low voltage silicon deployment. The current waveform shows very little distortion, suggesting high power factor values and low total harmonic distortion (THD).

Fig. 12 presents the PFC stage efficiency and total losses measured at both high line and low line with a 100W step load. The stage efficiency peaks around 99.05% at 230Vac and 98.1% at 115Vac. The efficiency curve is relatively flat and show very little roll-off at full power.

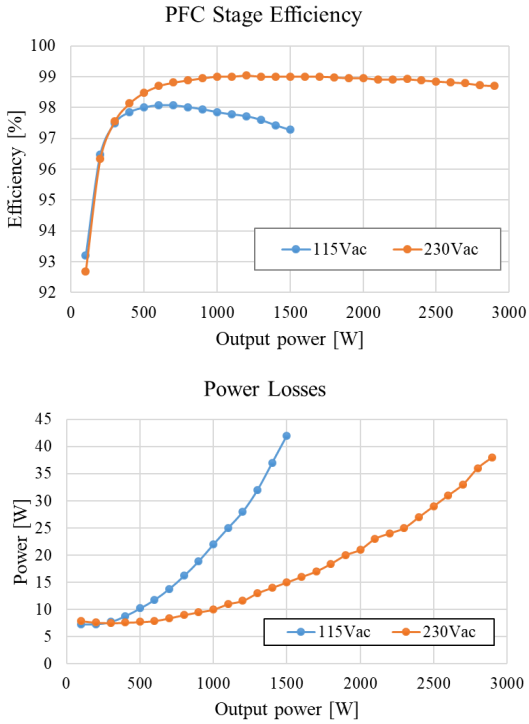


Fig. 12. 3kW PFC stage power loss and efficiency including EMI filter and 9V bias supply

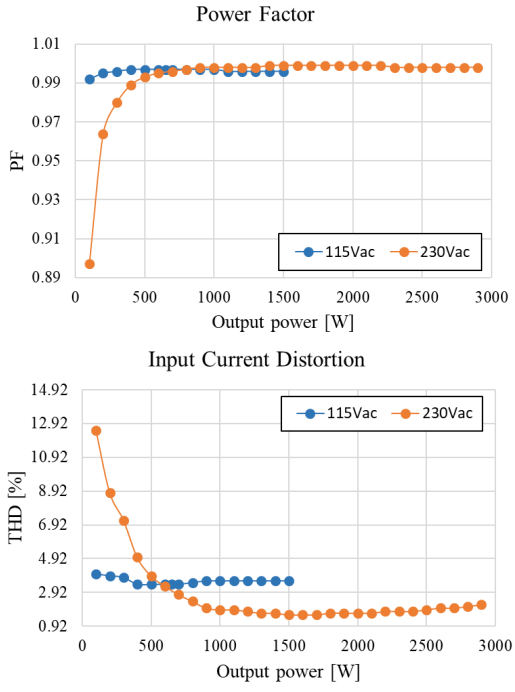


Fig. 13. Power factor and current THD of a 3-level bridgeless totem-pole PFC

The digital PFC controller has a current loop that is designed to adaptive its gain depending on inductance values. This helps maximize control bandwidth without compromising system stability. The outcome is high power factor, i.e. above 0.99, and low current distortion, i.e. below 5%, for 500W-3kW loads as demonstrated in Fig. 13.

Benchmarking performance and cost of the proposed 3-level implementation against conventional GaN-based bridgeless totem-pole PFC [16] is captured in TABLE IV. As can be seen, our solution offers comparable performance, but uses a lot smaller inductor and standard/multi-source/low-cost 150V MOSFETs for implementation. This helps keep the power train cost much lower and more affordable as compared to WBG technologies, which confirms that the objective of this study as highlighted in Fig. 2 is fully met.

TABLE IV. COST COMPARISON

	This study	**[16]**
Switching leg	8 x 150V 11mR MOSFETs	2 x 600V 35mR GaN
Synchronous rectification	2 x 19mR 650V MOSFETs	2 x 14mR 650V MOSFETs
PFC Inductor	40mm diamter & 28mm height	74mm diameter & 33mm height
Switching frequency	70kHz	65kHz
Efficiency	99%	99%
Power density	100W/in^3	-
Power train cost	Standard/Low	New product/High

VII. CONCLUSIONS

A low-cost yet ultra-high efficiency implementation of 3-level bridgeless totem pole PFC using series-connected 150V MOSFETs and precise isolated magnetic gate drivers is presented. The study confirms that established low-cost silicon can achieve better than 99% efficiency in CCM totem-pole PFC rectifiers as generally associated with WBG devices. Multilevel solutions also have sustainable competitive advantage in magnetics size (four-time reduction) and EMI/EMC performance, as well as an expected long-term cost advantage over conventional (2-level) WBG (SiC and GaN) -based implementation.

The paper also demonstrates that stacking low-voltage MOSFETs is key to performance maximization without penalizing system BOM cost and design complexity. Voltage sharing between two stacked devices can be achieved by precise isolated gate drive with minimal timing tolerance, i.e. less than 1ns delay matching. The proposed integrated control and drive card can make multilevel solutions practical and very cost effective for usage in high-volume AC/DC and DC/AC power conversion.

Many of the techniques discussed in this paper have parallel deployments in DC/AC and general energy management and these will be discussed in a future article.

Some of the technology and implementation details presented in this paper may be subject of patent applications.

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