400V SiC in Next-Generation 3-Level Flying Capacitor Bridgeless Totem-pole PFC

Rytis Beinarys
ICERGi Limited
Dublin, Ireland
rytisbeinarys@icergi.com

Seamus O'Driscoll
Tyndall National Institute
Cork, Ireland
seamus.odriscoll@tyndall.ie

***Abstract* — This paper proposes the design and implementation of a 3-level flying capacitor bridgeless totem-pole power factor correction (3L-FC-BTP-PFC) converter utilizing recently launched 400V Silicon Carbide (SiC) devices. It outlines key considerations and design challenges associated with adopting 400V SiC devices in place of a low-voltage series-connected silicon (Si) MOSFET arrangement. The proposed topology combines the benefits of a bridgeless totem-pole arrangement with the advantages of SiC technology. This combination enables superior performance in terms of higher efficiency, reduced gate driver complexity, increased system robustness, and enhanced power density. A comprehensive overview of the converter's operation, gate driver design, proposed power stage architecture, along with corresponding real-world experimental test results is presented.**

Keywords — silicon carbide (SiC), flying capacitor multilevel (FCML), low-cost isolated gate driver, hybrid flying capacitor voltage control, bridgeless totem-pole (BTP), power factor correction (PFC).

I. Introduction

As the demand for computational power in artificial intelligence (AI) applications continues to surge, server power supplies need to adapt to meet increasingly stringent industry requirements. Advanced GPUs are essential for AI training and are projected to require up to 3 kW per processor by the end of the decade. With AI server racks often housing multiple GPUs, the power supply unit (PSU) ratings are trending towards 8 kW and beyond [1]. This, in turn, drives the need for more efficient and robust power conversion solutions that can meet these requirements. With the recent announcement of the 400V CoolSiC™ MOSFET devices in the market [2], a significant advancement in multilevel power conversion systems can be achieved. Positioned between the existing 650V – 750V SiC device technology and the 150V – 200V Si MOSFET technology, 400V SiC switching devices in multilevel PFC design can offer a compelling balance of performance, cost, and design complexity. The evolution of power semiconductor technology has led to a paradigm shift in converter design, with increasing interest in adopting higher-voltage SiC MOSFETs to replace series-stacked low-voltage Si devices.

It is not uncommon to find series-connected Si MOSFETs utilized to achieve the necessary voltage handling capabilities in multilevel high-power applications [3], [4], but this approach introduces challenges such as increased circuit complexity, intricate voltage sharing mechanisms and higher switching losses due to higher component count in the power stage. On the other hand, the emergence of 400V SiC MOSFETs can address many of these limitations by offering superior material properties which allow for higher breakdown voltage, ultra-low switching losses, faster switching speeds and fast commutation robust diode properties. The outlined advantages can enable simplified designs, reduced component count and improved efficiency in multilevel power converter systems such as single phase 3L-FC-BTP-PFC (Fig. 1). However, transitioning to SiC technology introduces its own set of design considerations, such as managing higher dv/dt, ensuring robust gate drive arrangements, and addressing electromagnetic interference (EMI) challenges. This paper explores the transition from stacked low-voltage Si MOSFETs to 400V SiC devices, highlighting the benefits, considerations, and challenges in adopting this advanced technology.

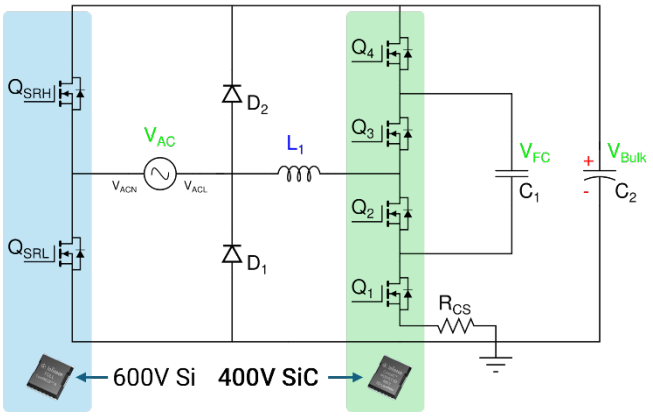

Fig. 1 Simplified circuit diagram of a 3L-FC-BTP-PFC utilizing 400V SiC MOSFET devices

II. Transitioning from 150V Si to 400V SiC in BTP-PFC: Design Challenges and Considerations

Well-known semiconductor manufacturers like *Infineon Technologies*, *Toshiba*, *Vishay,* etc., offer a wide range of moderate-frequency-capable Si MOSFETs primarily in the medium-voltage range (85V - 250V). However, 600V+ Si MOSFETs are generally limited to lower switching frequency applications such as synchronous rectifiers in PFC, solar inverters, etc. This is due to the large gate charge (Q_G) and poor reverse recovery performance (Q_{rr}) due to its slow intrinsic body diodes. While 600V – 750V SiC devices offer superior performance [5], they are not a viable solution in such cases due to their significantly larger V_{DS} rating which leads to unnecessarily increased system cost. This is where the recently announced 400V SiC devices from *Infineon Technologies* perfectly position themselves. It offers the ideal balance of high efficiency, fast switching capabilities and optimized cost for such applications.

Table-I highlights some of the key parameters of 150V Si and 400V SiC MOSFET technology. The comparison is carried out between 2x 150V Si FETs (BSC093N15NS5) and a single 400V SiC MOSFET (IMT40R025M2H).

TABLE I. 150V SI MOSFETS VS 400V SIC MOSFET COMPARISON

Parameter	*2x 150V Si*	*1x 400V SiC*
Voltage blocking (V_{DS})	300V	400V
Reverse recovery charge (Q_{rr})	High	Extremely low
Switching speed (f_{sw})	Moderate	Faster
Thermal resistance (R_{th})	Higher	Lower
Gate driver design[a]	Complex	Simpler
Conduction losses ($T_j = 100°$)	Moderate	Moderate
Component Cost[b]	Lower	Higher

[a.] Number of gate driver circuits and the PCB layout

[b.] Cost based on 1,000 units from global component distributors

Considering the numerous advantages that SiC technology brings, the benefits far outweigh the higher initial cost per device. Additionally, since multilevel converters are typically used in medium- to high-power designs, where cost sensitivity is not as stringent, 400V SiC technology seems to be a perfect fit for the adoption.

III. OVERVIEW OF ADVANCED 3L-FC-BTP-PFC CONVERTER

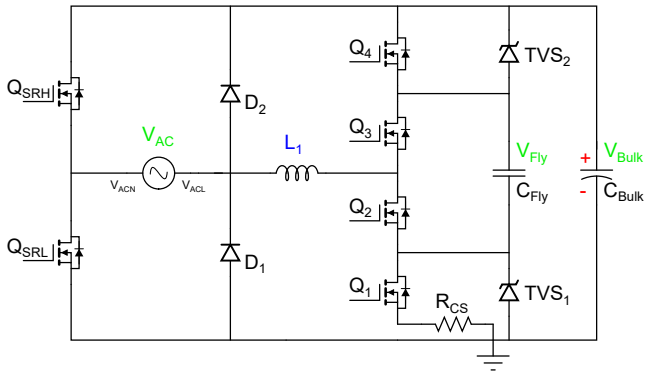

Fig. 2 Circuit diagram of 3L-FC-BTP-PFC with TVS diodes

Consider a simplified circuit of 3L-FC-BTP-PFC depicted in Fig. 2 above. The converter arrangement consists of the following components:

- Synchronous rectifier MOSFETs Q_{SRL} and Q_{SRH}.
- A pair of inrush current diodes D_1 and D_2, utilized exclusively during startup and latch up modes.
- The main PFC inductor L_1.
- HF boost leg with SiC MOSFETs Q_1, Q_2, Q_3, Q_4.
- Transient voltage suppressors TVS_1 and TVS_2 for flying capacitor initialization and protection.
- Additional flying capacitor C_{Fly} for voltage division and the output capacitor C_{Bulk}.
- Simple and cost-effective shunt-type pulsed inductor current sense resistor R_{CS}.

A. *Control Technique: Phase Shift Modulation (PSM)*

The HF string of SiC MOSFETs Q_{1-4} is controlled using a phase-shift modulation (PSM) in which devices Q_1 and Q_4 make up an outer phase and are driven in complementary fashion. The same applies to switches Q_2 and Q_3 forming an inner phase with an offset of 180°. The proposed modulation scheme allows for the flying capacitor voltage to track the reference voltage of $V_{bulk}/2$. During steady-state operation with a nominal PFC output voltage of 400V, each SiC MOSFET experiences a blocking voltage of approximately 200V. This occurs provided that the natural charge balance condition of the flying capacitor is satisfied.

B. *Switching Frequency Control*

The block diagram in Fig. 3 illustrates a variable switching frequency control architecture of a digital PFC controller. Central to this system is an ARM Cortex M0+ based microcontroller which encapsulates software defined control algorithms. Other key functional blocks include auxiliary voltage sense amplifiers for voltage measurement, isolated self-powered gate drivers and a switched-gain current sense amplifier to dynamically adapt current sensing based on the input current magnitude. This configuration allows for a reduced converter switching frequency, thereby minimizing switching losses and reducing the required drive power. The result is an optimized PFC system that achieves a balance between energy efficiency and improved current sense measurement accuracy at light to medium load operating conditions.

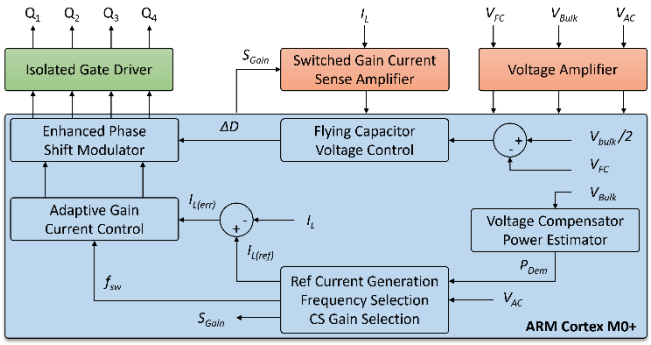

Fig. 3 Digital frequency control block diagram for 3L-BTP-PFC

C. *Hybrid Flying Capacitor Voltage Balance Control and Pre-charge Mechanism*

In the context of FCML power conversion systems, additional care must be taken to ensure that flying capacitor(s) charge balance is not compromised during high energy transient events such as start-up or input voltage surge. In addition, unbalanced voltage can occur during steady-state operation due to device tolerances, digital control timing delay, and hardware layout parasitic elements. The proposed hybrid flying capacitor voltage control is a simplified variant of the method which is employed in stacked 150V switching device PFC design [6]. The passive voltage balance enforcement circuitry requires only 2 additional components, namely TVS_1 and TVS_2 while the active part of it remained unchanged.

In this arrangement, TVS devices serve a secondary purpose, functioning as a flying capacitor voltage initialization mechanism during the power-up phase of the PFC converter. However, it is crucial to select the voltage

clamping components carefully to ensure that the PFC converter operates without any adverse effects during both startup and steady-state conditions. In an ideal scenario, the TVS diodes should facilitate pre-charging of the flying capacitor to approximately half of the output voltage during the start-up sequence, while also assisting the outer SiC MOSFETs Q1 and Q4 in clamping excess energy during input voltage surges. However, with the nominal blocking voltage of each SiC MOSFET during steady-state operation of around 200V (just 50% of their V_{DS} rating) it becomes challenging to optimize the TVS diodes for both functions simultaneously. If TVS diodes with a breakdown voltage V_{BR} are selected close to $V_{Bulk}/2$, careful consideration must be given to their maximum peak pulse power (P_{PPM}) rating. These diodes will handle the bulk of the energy dissipation during critical events, such as the soft-start sequence and input voltage surges. Ensuring that P_{PPM} is sufficiently high to withstand these transient conditions is essential to prevent excess thermal stress and potential failure. However, with ICERGi's proprietary, fast (<20 µs) input voltage surge protection mechanism [7], the excellent pulsed avalanche energy handling capabilities of SiC MOSFETs, and a slightly overdesigned flying capacitor bank, alternative strategies can be employed to achieve the flying capacitor voltage pre-charge during startup.

IV. Isolated Gate Driver Design

The shift from Si to SiC MOSFETs in the magnetically coupled floating gate driver circuit requires a thorough redesign to accommodate the distinct characteristics of SiC technology. While the switching profile for a SiC MOSFET is relatively similar to a Si MOSFET [8], several gate driver design challenges arise. First, SiC MOSFETs require a higher V_{GS}. The recommended unipolar gate drive voltage for 400V SiC is 18V, which is higher than the typical 12V used for Si devices. Second, achieving faster charge and discharge rates of the gate capacitances is essential to support high-speed switching. To satisfy these requirements, redesigning planar transformers is necessary. This process requires adjusting the turns ratio of the primary and secondary windings as well as resizing the PCB tracks. Moreover, the width of the primary side drive pulse must be carefully tuned to account for the external turn-on ($R_{ON,ext}$) and turn-off ($R_{OFF,ext}$)gate resistor values to achieve a slightly underdamped V_{GS} with minimal overshoots/undershoots during both turn-on and turn-off transitions. Precise dead time insertion (ideally variable) is also essential in this hard-switched topology to prevent shoot-through currents and enable reliable switching transitions.

A. Planar Transformer Implementation

The 400V CoolSiC™ MOSFETs can be reliably driven with a unipolar drive voltage (0 – 18V) and does not require a negative turn-off drive voltage. The isolated gate driver transformer design consists of a single primary winding (2 turns) and two secondary windings for each SiC device: the turn-on winding (4 turns) and the turn-off winding (1 turn). Note, a logic-level pulse of 2V is sufficient to reliably pull the gate down to almost 0V during turn-off. The transformer turns ratio can be described by the following expression:

$$N_{\mathrm{p}} : N_{\mathrm{s(on)}} : N_{s(off)} = 2:4:1 \qquad (1)$$

With a primary side voltage ranging from 9V to 10V and the specified transformer turns ratios, both transitions can be satisfied based on the following expressions.

Turn-on:

$$V_{\mathrm{p}} * \frac{N_{\mathrm{s(on)}}}{N_p} \geq V_{S(on)} \rightarrow 9V * \frac{4}{2} \geq 18V \qquad (2)$$

Turn-off:

$$V_{\mathrm{p}} * \frac{N_{\mathrm{s(off)}}}{N_p} \geq V_{S(off)} \rightarrow 9V * \frac{1}{2} \geq 2V \qquad (3)$$

By reducing the number of FETs in boost leg from 8x 150V to 4x 400V SiC, a 4-layer PCB stack-up is sufficient to implement planar transformer windings. However, a 6-layer stack-up was used instead to test several winding constructions for both the primary and secondary sides. For all windings, the selected track width and gap are 0.10 mm and 0.15 mm, respectively. The primary-side windings are placed on external layers to handle the larger primary current. The secondary-side turn-on and turn-off windings are placed on four inner layers. To ensure strong magnetic coupling and minimize interwinding capacitance, the windings are routed with minimal interlayer overlap. Additionally, the top three layers and bottom three layers are designed symmetrically to provide greater flexibility in configuring the gate driver circuit, regardless of which side of the PCB it is placed on.

B. Gate Driver Optimisation

To accurately capture no-load switching transients of the SiC MOSFETs, waveforms were captured using a 200 MHz bandwidth, with measurements taken near the device terminals to accurately reflect gate drive loop behaviour and minimize parasitic influences. Test setup and some of the key parameters are outlined in Table-II. Based on Fig. 5, the tight gate drive loop with low parasitic inductance ensures that no substantial drive-on or drive-off oscillations are present at the drive terminals of each SiC device Fig. 4. However, more insightful test results can be obtained by measuring V_{GS} during PFC operating mode. Specifically, examining the floating gate drive waveforms which are crucial to verify that there are no parasitic turn-on events during hard-switched transitions.

TABLE II. Gate Driver Optimisation Parameters and Setup

Item	***Value***	***Description***
SiC MOSFET	IMT40R015M2H[a]	$400V, 111A\ (T_c), 15\ m\Omega$
Isolated Gate Driver	IC70-001	$20V, 2A\ (I_{sink}), 4\ A\ (I_{src})$
Transformer Core	EE7.3B	$R10KC$
Parameter	***Value***	***Description***
f_{sw}	65.2 kHz	Switching frequency
V_p	9V – 10V	Primary side voltage
$V_{\mathrm{s}\ (on)}$	16V – 18V	Secondary side voltage
D	3.8%	Duty ratio
T_{pulse}	85ns – 165ns	Turn-on/-off pulse

[a.] Benchmark was carried out on a 15 mΩ component

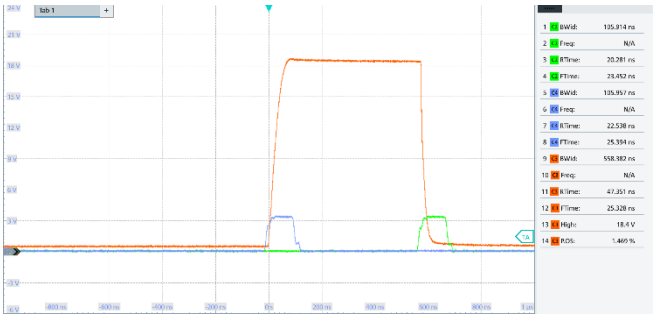

Fig. 4 Test conditions: $R_{ON} = 3.3\ \Omega, R_{OFF} = 2.2\ \Omega, T_{pulse} = 105\ ns, V_{pri} = 9V$ (V_{GS}, $T_{pulse(on)}$, $T_{pulse(off)}$)

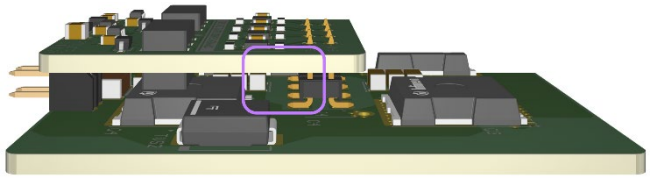

Fig. 5 Side profile of PFC control and boost leg power board assembly (area associated with the gate drive loop for Q_4)

The estimated gate driver loop inductances for the modular design shown in Fig. 5 ranges from 10 nH to 12 nH.

C. Potential Improvements

Several design changes can be adopted to enhance the gate driver design. To minimize parasitic gate drive loop inductance further and to optimize the circuit layout:

- Remove SMD connector from the gate drive loop which in turn can reduce the parasitic loop inductance in the order of several nH.
- Place gate drivers closer to the transistor devices to allow for even faster switching transitions.
- Widen and/or overlap the return path of the gate driver traces with the corresponding signal traces to significantly reduce parasitic inductance and minimize loop area.

V. Hardware Design for Technology Demonstration

To evaluate and validate the adoption of 400V CoolSiC™ devices in multilevel PFC, 3.3 kW 3L-FC-BTP PFC prototype was designed and assembled (Fig. 6). The corresponding BOM of the design is presented in Table-III. Note that only some of the key components are listed.

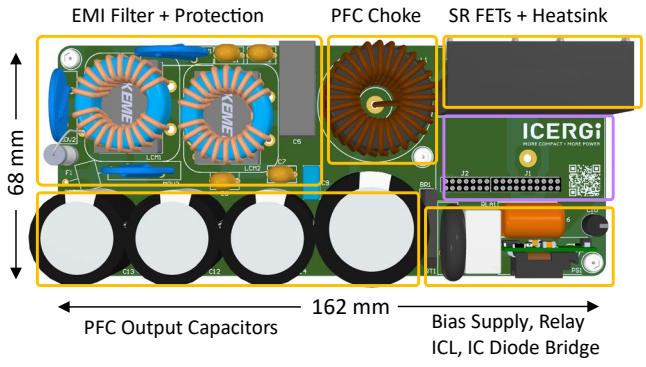

Fig. 6 3.3kW SiC-based 3L-BTP-PFC main board (area for the digital PFC module connection)

TABLE III. 3K3W SiC-Based PFC Bill of Materials (BOM)

Component	*Name*	*Description*	*Qty*
Power Stage	C_{Bulk}	470µF 450V output capacitors	3
	$C_{Fly(1)}$ $C_{Fly(2)}$	4.7µF 450V (film) FCs 68 nF 500V X7R (ceramic) FCs	2 6
	L_1	250µH inductor (MS109125-2)	2
	Q_{1-4}	400V 25mΩ HF SiC MOSFETs	4
	$Q_{SRL/H}$	600V 16mΩ SR MOSFETs	2
Input Protection	MOV_1 F_1 GDT	430V 8kA varistor (20 mm) 20A 600VAC/500VDC fuse 600V 15kA gas discharge tube[c]	3 1 1
EMI Filter	C_{X1-2} C_{X3} C_{Y1-4} L_{com1-2}	1µF 310V_{AC} X – capacitor 1.5µF 310V_{AC} X – capacitor 470pF 310V_{AC} Y – capacitor 2mH common mode choke (16A)	2 1 4 2

The Digital PFC module hardware prototype is comprised of a control daughterboard and a power card that houses 4x IMT40R025M2H SiC devices (Fig. 7). A 45x45x20 mm heatsink is attached to the module to provide efficient bottom-side PCB cooling for all SiC devices.

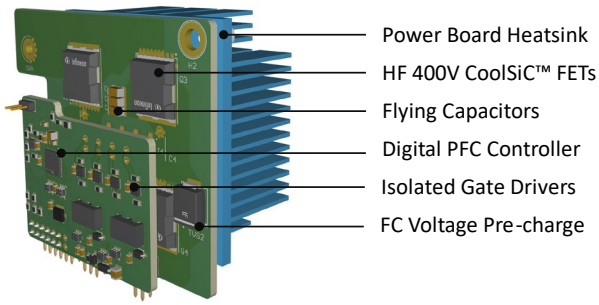

Fig. 7 Digital PFC module prototype (*Note: Film-type flying capacitors are not shown*)

In the design phase of the 3L-FC-type boost leg, particular attention was paid to the layout and minimizing both the inner and the outer power loop areas. Poor design can lead to significant drain-source (V_{DS}) overshoots and failure to pass relevant conducted EMI standards.

VI. Experimental Results

To validate the 3L-FC-BTP-PFC performance with 400V SiC devices, experimental results were collected with primary focus on efficiency metrics and operational behaviour. Waveforms during both startup (Fig. 8) and steady-state (Fig. 9) operations were captured and analysed.

A. Experimental Waveforms

During the startup of the PFC, close to the worst-case scenario is tested with $V_{IN} = 265V_{AC}$ and a phase angle near 90°. The flying capacitors are pre-charged to 140V, which is close to $V_{Bulk}/2$, thereby minimizing capacitor inrush current before the converter transitions to boost mode operation. Note that all waveforms have a 20 MHz bandwidth limit applied to each channel for clarity. Input and PFC choke currents are shown as 10V/div and 5V/div but should be interpreted as A/div instead.

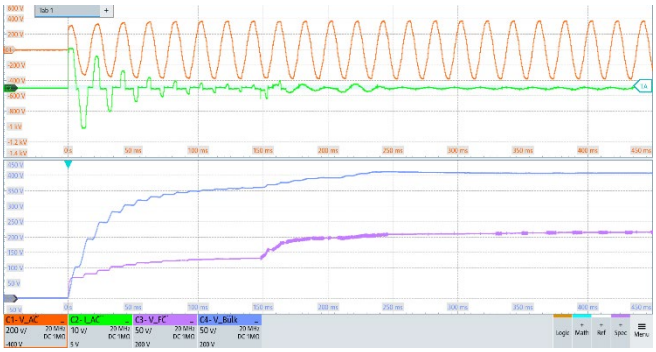

Fig. 8 Start-up sequence with flying capacitor voltage initialization ($V_{IN} = 265V_{AC}, P_{OUT} = 0W$)

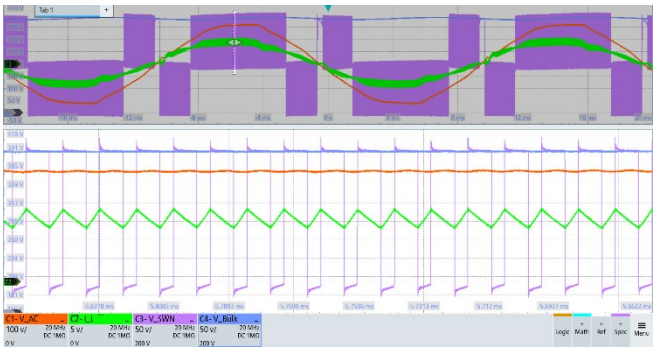

Fig. 9 Steady-state operation ($V_{IN} = 230V_{AC}, V_{OUT} = 385V_{DC}$, $f_{sw} = 45.8\ kHz,\ P_{OUT} = 50\%$)

B. Converter Efficiency

The PFC efficiency data outlined in Fig. 10 is measured up to 1650W using IMT40R025M2H SiC devices. It demonstrates peak efficiency exceeding 99.2%, with potential for further optimization. The efficiency measurements include both the two-stage line filter and the 12V bias supply but exclude the external DC fan. The converter was tested in an open-frame configuration. Natural convection was used for $V_{IN} = 230V_{AC}$, while $V_{IN} = 115V_{AC}$ had an approximate airflow of $0.34m^3/min$ (12 CFM).

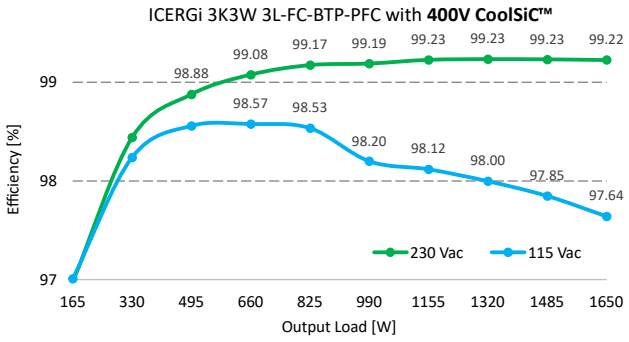

Fig. 10 PFC efficiency up to 1650W with IMT40R025M2H SiC

VII. Conclusion

In conclusion, the successful development of ICERGi's SiC gate drive solution has demonstrated robust gate driver capabilities. This achievement allows for a significant advancement in the multilevel power converter sector through the integration of 400V SiC technology, proprietary digital control, and proven gate drive techniques. The presented experimental results validate the successful integration and adoption of 400V SiC MOSFETs in a 3L-FC-BTP PFC applications. As a result, greater power density, simplified gate driver design, and enhanced reliability can be achieved, particularly in medium- to high-power single-phase PFC applications.

Some of the technological aspects and implementation details covered in this paper may be the subject of patent applications.

Acknowledgment

This material is based upon works supported by the Department of Enterprise, Trade and Employment and Enterprise Ireland through the Irish Government's Disruptive Technology Innovation Fund (Grant No. DT2020-0222).

References

[1] S. Daryanani, "Improvements in Performance and Voltage Range of SiC MOSFETs," *Power Electronics News,* pp. 4-6, 2024.

[2] "400 V CoolSiC™ AI server deepdive," Infineon, 2024.

[3] P. B. G. Mostafa Khazraei, "Five-level Active Neutral Point Clamped Flying Capacitor Inverter Design Based on OptiMOS™ 5 150 V," Infineon Technologies AG, Munich, Germany, 2020.

[4] R. Beinarys, S. O'Driscoll and T. T. Vu, "Flying Capacitor Voltage Imbalance Protection in Multilevel Bidirectional Inverters during Surge," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, 2023.

[5] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," in *IEEE Transactions on Industrial Electronics*, 2017.

[6] T. T. V. Rytis Beinarys, "Hybrid Voltage Balancing Control in 3-level Bridgeless Totem-pole PFC," in *Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA, 2021.

[7] T. T. V. George Young, "Method of Controlling a Current Shaping Circuit in a Converter with Power Factor Correction". United States of America Patent US10944318B2, 26 March 2020.

[8] O. S. Corporation, "SiC MOSFETs: Gate Drive Optimization," 2023.

[9] D. Miller, "Surge Immunity Test Analysis for Modern Switching Mode Power Supplies," in *International Telecommunications Energy Conference (INTELEC)*, Austin, TX, USA, 2016.